1kW GaN *S* Band Radar Transistor

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***Abstract*—This paper describes a GaN transistor with 1kW output power for *S* band radar and other applications. This is believed to be the highest power ever reported from a single-ended transistor at this frequency and is a threefold improvement on the previous best.**

Keywords—GaN; transistor; S band; radar

I. INTRODUCTION

Silicon bipolar transistors for *S* band radar have been available for many years and will continue to be available for many years to come. This technology is proven, highly reliable, and offers high efficiency due to the use of class C bias, typically around 50%. Furthermore, bipolar transistors have the simplest form of DC bias networks of any transistor technology at this frequency range and use the least number of additional components on the RF circuit board. However, the technology has three distinct disadvantages, namely low RF gain (typically around 9dB for the highest power parts), high output capacitance per Watt which imposes a power/bandwidth limit on the technology, and the need for an insulating material in the package, typically BeO but sometimes AlN. The low RF gain is a result of using emitter ballast resistors. These are required to prevent thermal run-away but they also provide negative feedback which lowers the intrinsic gain of the transistor. An example of a typical state of the art product is IB2729M170 [1] which delivers typically a minimum pulsed output power of 190W over 2.7-2.9GHz with 45% power-added efficiency and >9dB gain.

More recently, LDMOS has been developed for *S* band radar applications. The main advantage of LDMOS is that it uses a non-insulating package which doesn't require an environmentally unfriendly material such as BeO. It also offers slightly higher gain, typically 2dB more for the same output power as a bipolar equivalent, but the maximum output power is about the same for the two technologies. LDMOS devices are typically designed for Class A/B operation which has worse efficiency than Class C (typically 5% less), and the MOSFET device requires additional DC bias circuitry to suppress the low frequency oscillations coming from the bias networks. In order to design a RF test circuit that is free from spurious oscillations both the gate and the drain terminals need many external components such as ferrite beads and an array of decoupling capacitors on the DC bias feeds from the DC power supplies. In summary, LDMOS hasn't provided the radar designer with a huge leap forward in performance. Due to the frequency limitations of silicon technology there is little prospect of any future significant improvement in either bipolar or LDMOS performance at *S* band. An example of a typical state of the art LDMOS transistor is ILD2731M140 [2] which delivers typically a minimum pulsed output power of 180W over 2.7-3.1GHz with 40.5% power-added efficiency and >10dB gain.

GaN transistors, on the other hand, offer a quantum leap forward in performance. GaN is a wide band-gap semiconductor and this enables the use of a much higher supply voltage (50V versus 32V for LDMOS) which, in turn, results in much higher power density. The high power density provides lower capacitance per Watt which enables higher power parts to be produced for the same bandwidth. The higher supply voltage also means that the load resistance is higher for the same output power which results in higher efficiency and easier circuit design. However, the higher power density creates heat dissipation problems which are a serious issue for CW parts but which makes GaN an ideal technology for high power pulsed applications. Table 1 summarizes the typical performance of 2.7-2.9GHz transistors designed for 10% duty cycle 300µs pulse lengths with broadly similar output power. The GaN device in this case is operated at a similar supply voltage rather than one to maximize power, efficiency and gain.

TABLE I. TRANSISTOR COMPARISON

Device	Parameter				
	Technology	*Power (W)*	*Power-Added Efficiency %*	*Gain (dB)*	*Voltage (V)*
IB2729M170	Si Bipolar	190	45	9.5	36
ILD2731M140	LDMOS	180	40.5	10.5	32
IGN2729M250 [3]	GaN	260	51	9.5	36

In 2011 Kwack *et al* [4] reported a 1kW amplifier for 2.9-3.3GHz radar applications that combined 8 approximately 150W GaN transistors to achieve the 1kW output power. The

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output stage occupies an area of around 160 cm^2 after subtracting the area occupied by the 4 isolators. In this paper a single GaN transistor is reported that delivers 1kW peak at the center frequency of 2.8GHz with a minimum of 56% power-added efficiency and 10dB gain. This removes the need to use a total of 10 Wilkinson power combiners, and the total circuit area is 32 cm^2 - less than $1/5^{th}$ of that required by Kwack *et al.* To the best of the authors' knowledge this represents the highest power achieved from a transistor at this frequency and sets a new bench-mark for solid-state in terms of the overall combination of power, gain and efficiency.

II. TRANSISTOR DESIGN AND PERFORMANCE

A. *Die Design*

Integra manufactures GaN transistor die on a 4" SiC substrate. The gate length is 0.5µm and the die uses via holes for source grounding. As the transistors are designed for pulsed operation the die are optimized for high drain-source breakdown voltage so that a 50V supply voltage can reliably be used. The largest die design in production is an AlGaN/GaN-on-SiC HEMT with 36mm total gate periphery. Each die is capable of over 150W output power over the 2.7-2.9 GHz band, and the 1kW part described in this paper uses 7 of these dice. The die has been designed to ensure low thermal resistance with a two-prong approach: 1) the SiC substrate is thinned down to 3 mil thickness, and 2) the die pitch is 30µm wide which allows heat dissipation through the SiC substrate and also allow enough width for the Au-based source and drain metal fingers for low electro-migration and high long-term reliability. The die technology relies on Integra's proven 0.5µm gate length AlGaN/GaN HEMT with double field plate design and extensive gate-drain drift region length for negligible DC-RF dispersion at 50V nominal bias operation. An SEM cross section of the die around the gate region is shown in Fig. 1.

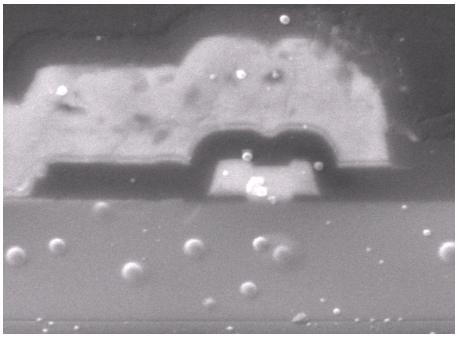

Fig. 1 – SEM cross-section of Integra's 0.5µm GaN HEMT chip with double field plate design.

The double field plate design features a first field plate through a T-shaped gate with 0.5µm gate foot length formed by etching the 1^{st} silicon nitride passivation layer, and a raised gate over-hang on top of the silicon nitride passivation layer. This shape of the gate is achieved through the same metallization layer, and it also offers reduced gate resistance for high frequency operation. The second field plate is connected to the grounded source finger inside the active area, and wraps around the gate to reduce feedback (drain-gate) capacitance while at the same time reducing output conductance drain modulation. The combination of the two field plates results in lower electric fields at the surface of the GaN epi-layers and the silicon nitride passivation layer, minimizing trapping and de-trapping effects occurring at the interface. Source and drain fingers use 3µm thick Au-plated metallization for superior electro-migration capability and low series resistance across the finger's 300µm width.

The AlGaN/GaN HEMT transistor uses Integra Technologies' proprietary epi-layer design and is built with a well-established and mature process. Ohmic contacts are made of a Ti/Al/Ni/Au stack annealed in a short and high-temperature RTP step. A triple ion-implantation step is used for device isolation. Surface passivation, which is a very critical step for obtaining a DC-RF dispersion-free GaN HEMT technology, is accomplished by PECVD low-stress silicon nitride deposition. A 0.5µm gate length is then formed by a low-damage silicon nitride etch step, followed by a 0.5 µm thick Ni/Au gate metal stack e-beam deposition that forms both the 0.5 µm gate minimum feature and the gate-connected field plate. Another silicon nitride deposition step is used for isolation between the gate field plate and the next source connected field plate. The second field plate layer is formed with another e-beam Au-based metal layer that also adds metal on top of the source and drain ohmic contacts for lower contact resistance. The final steps of the front-side process include the formation of air bridges and 3 µm thick plated Au for the source and drain fingers, as well as the wire bonding pads. Wafer processing is completed after back-grinding the SiC substrate to a 3-mil thickness and another 3 µm plated Au back metal deposition. The die is attached to the package flange with a AuSn pre-form at 330 °C. A picture of the die with 36mm gate periphery is shown in Fig. 2. Each gate finger is 300µm long. The unit cell of 0.6mm gate periphery (2 gates) is 60µm wide, and the 36mm die consists of 60 cells. The die is 154 mils x 40 mils in size.

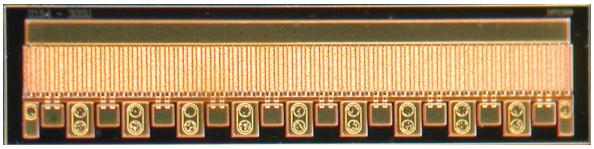

Fig. 2 – Picture of Integra's 36mm gate periphery 0.5µm GaN HEMT die.

The typical pinch-off gate voltage is -3.5V, and the typical gate-drain reverse voltage breakdown exceeds a minimum of 150V for safe and reliable operation at 50V.

B. *Transistor Design*

Figure 3 is a photograph of the transistor. Although the transistor uses a push-pull package the two halves of the device are connected together on the printed circuit board so that the device is operated in a single-ended configuration. Internal pre-

matching is used within the package and Table 2 shows how effective this is in raising the impedance to a manageable level even though this is a 1kW transistor. The corresponding impedance values for a 1kW 1030MHz spot frequency LDMOS transistor are also shown as well to demonstrate how beneficial the lower capacitance per Watt of GaN is in keeping the impedance higher and this equates to less loss in the output matching network and hence higher efficiency.

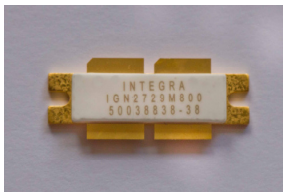

Fig. 3 – Picture of 1kW pulsed transistor

TABLE II. TRANSISTOR OPTIMUM SOURCE AND LOAD IMPEDANCES

Device	Parameter		
	Frequency (GHz)	*ZSopt (Ω)*	*ZLopt (Ω)*
IGN2729M800	2.7	1.6 + j2.2	1.4 – j3.1
	2.8	1.6 + j2.4	1.5 + j3.9
	2.9	1.8 + j2.7	2.8 + j6.2
ILD1011M1000HV	1.03	0.86 + j0.34	0.30 + j0.40

C. *Transistor Performance*

Figures 4, 5 and 6 show the measured power output versus power input, efficiency versus power output, and gain versus power output, respectively. The measured data is obtained in a fixed-tuned circuit with a supply voltage of 50V and a quiescent current of 100mA. The pulse width and duty cycle are 300µs and 10%, respectively. The output power peaks at just over 1kW with an associated gain of 11dB and 56% power-added efficiency.

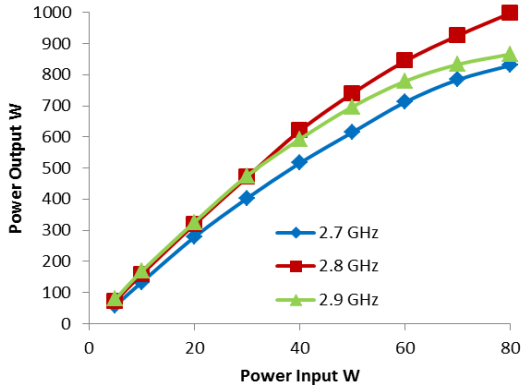

Fig. 4 – Output power vs input power.

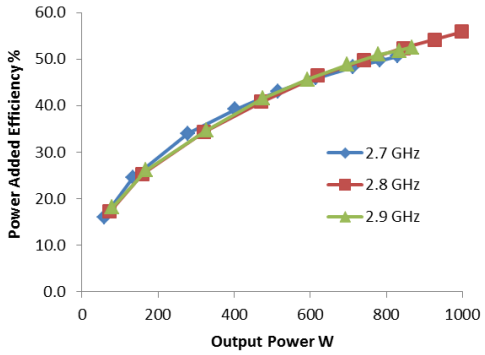

Fig. 5 – Power Added Efficiency vs output power.

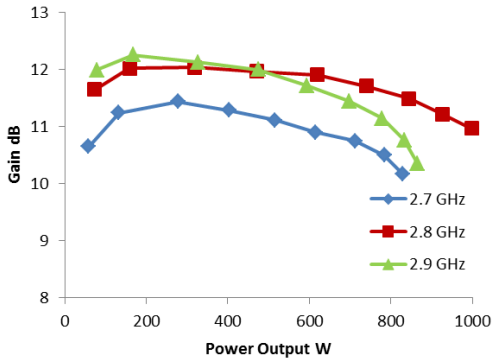

Fig. 6 – Gain vs Output power.

Figure 7 shows output power and efficiency as a function of drain voltage at 2.9GHz. It can be seen that the efficiency is not a sensitive function of drain voltage and remains almost constant over the drain voltage range of 40-50V. Also, the output power is almost a linear function of supply voltage over a 6dB range of output power which facilitates AGC.

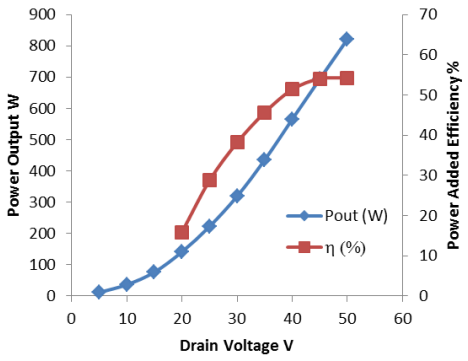

Fig. 7 – Output power and power added efficiency as a function of drain voltage.

The thermal performance of a transistor is a critical parameter in many applications and Table 3 shows the measured pulse droop. For pulse lengths >200 µs the heating that occurs during the pulse causes pulse droop which becomes more pronounced as the pulse length increases, but for short pulse lengths and low duty cycles there is negligible pulse droop. The peak transient thermal resistance is 0.13^0C/W.

TABLE III. PULSE DROOP PERFORMANCE

Pulse Length µs	Duty Cycle %	Pulse Droop dB
10	1	+0.07
10	10	+0.06
100	10	-0.08
200	10	-0.17
300	10	-0.22
500	10	-0.31
1000	10	-0.46

An issue of great concern in practical applications is VSWR withstand capability. A large external VSWR mismatch would undoubtedly cause device failure. By running VSWR mismatch tests at varying duty cycle it is readily demonstrated that VSWR withstand capability decreases as duty cycle increases which demonstrates that the failure mechanism is thermal in origin. In this respect, GaN devices operated at maximum peak output power are less robust than many LDMOS devices which are often designed to be capable of operating under CW conditions whereas this GaN device can only deliver 1kW under pulsed operation. However, it is possible to protect the device from a high VSWR by incorporating a circulator at the output. However, there is an additional issue which must also be addressed, namely a moderate external VSWR that may be too small to cause device failure might be sufficiently large to cause the device to oscillate or exhibit pulse break-up. This transistor has been shown to be stable up to 3:1 VSWR.

III. CONCLUSIONS AND FUTURE WORK

This paper has reported the performance of a 1kW *S* band single-ended radar transistor that has set a new bench-mark for transistors operating in this frequency range. Although this paper has focused on radar applications, this transistor can also be used in Linear Accelerator applications operating at 2.856GHz as well as medical applications such as Radio Frequency Ablation (RFA) used in cancer treatment. This 1kW single-ended transistor used a push-pull package for convenience with the two halves connected in parallel on the RF circuit. Finally, due to the high value of the external impedances as shown in Table 2, it is technically feasible to extend the bandwidth to at least 2.7-3.1GHz, and possibly even wider, at around the 1kW level.

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