

60W AVIONICS LDMOS

The high power transistor part number ILD0912M60 is designed for the frequency band 960-1215 MHz. Operating at 10us/10% pulse conditions this LDMOS FET device supplies a minimum of 60 watts of power across the instantaneous operating bandwidth of 960-1215 MHz. All devices are 100% screened for large signal RF parameters.



Silicon LDMOS FET

- High Power Gain
- Superior thermal stability

Class AB Operation

- Gate biased to $I_{DQ} = 550 \text{ mA}$

Configuration

- Common Source

Gold Metal

- Maximum Reliability

Package

- Thermally enhanced
- Pb-free and RoHS-compliant

Epoxy Sealed Lid

- Gross Leak Qualified

RF Test Fixture

- Broadband
- Matched to 50Ω
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning required

TYPICAL DATA TYPICAL DATA TYPICAL DATA TYPICAL DATA

Freq (MHz)	P_{IN} (W)	RL (dB)	P_{out} (W)	G_p (dB)	G_f (dB)	I_d (A)	η_d (%)	Droop (dB)	VSWR - LMT 3:1 (P-F)
960	1.4	-18.0	60	16.41		8.600	64.5	0.14	P
1090	1.4	-17.0	60	16.48	0.85	8.610	64.3	0.07	P
1215	1.6	-18.0	60	15.63		8.700	62.5	0.03	P

MAXIMUM RATINGS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Drain-Source Voltage	V_{DS}	--	65	V	--
BD	Gate-Source Voltage	V_{GS}	-0.5	12	V	--
BD	Storage Temperature Range	T_{STG}	-40	+150	°C	--
BD	Operating Junction Temperature Range	T_J	-55	+200	°C	--
Note	Screen 'BD' = parameter qualified By Design.					

THERMAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	0.17	°C/W	$V_{DS}=30V, I_{DQ}=550mA, T_F=25\pm5^\circ C, P_{OUT}=60W, 10\mu s/10\%$.
Note	Screen 'BD' = parameter qualified By Design.					

PROCESSING SPECIFICATIONS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

DC ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Drain-Source Breakdown Voltage	BV_{DSS}	65	--	V	$I_D = 10mA, V_{GS} = 0V, T_F = 25\pm5^\circ C$
100%	Drain Leakage Current	I_{DSS}	--	2	μA	$V_{DS} = 30V, V_{GS} = 0V, T_F = 25\pm5^\circ C$
100%	Gate Threshold Voltage	V_{GSTH}	1.5	5.25	V	$I_{DQ} = 100mA, V_{DS} = 5V, T_F = 25\pm5^\circ C$
100%	Gate Leakage Current	I_{GSS}	--	1	μA	$V_{GS} = 5V, V_{DS} = 0V, T_F = 25\pm5^\circ C$

RF ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	RL	-18	-10	dB	$V_d=30V, P_{OUT} = 60W, 10\mu s, 10\%, I_{dq}=550mA, T_F=25\pm 5^\circ C, F=F1, F2, F3.$
100%	Input Power	Pin	0.95	1.69	W	$V_d=30V, P_{OUT} = 60W, 10\mu s, 10\%, I_{dq}=550mA, T_F=25\pm 5^\circ C, F=F1, F2, F3.$
100%	Power Gain	G_p	15.5	18	dB	$V_d=30V, P_{OUT} = 60W, 10\mu s, 10\%, I_{dq}=550mA, T_F=25\pm 5^\circ C, F=F1, F2, F3.$
100%	Drain Efficiency	N_d	42	100	%	$V_d=30V, P_{OUT} = 60W, 10\mu s, 10\%, I_{dq}=550mA, T_F=25\pm 5^\circ C, F=F1, F2, F3.$
100%	Load Mismatch Tolerance	VSWR-LMT	3:1	--	--	$V_d=30V, P_{OUT} = 60W, 10\mu s, 10\%, I_{dq}=550mA, T_F=25\pm 5^\circ C, F=F1, F2, F3,$ Rotate 3:1 output VSWR through 360° phase. Survival.
100%	Gain Flatness	GF	--	2.5 dB	dB	$V_d=30V, P_{OUT} = 60W, 10\mu s, 10\%, I_{dq}=550mA, T_F=25\pm 5^\circ C, F=F1, F2, F3.$
100%	Signal Amplitude Droop	Droop	-0.5	0.5	dB	$V_d=30V, P_{OUT} = 60W, 10\mu s, 10\%, I_{dq}=550mA, T_F=25\pm 5^\circ C, F=F1, F2, F3.$
Note 1	F1= 960 MHz, F2= 1090 MHz, F3= 1215 MHz.					
Note 2	T_F = Device flange temperature.					
Note 3	Screen 'BD' = parameter qualified By Design.					

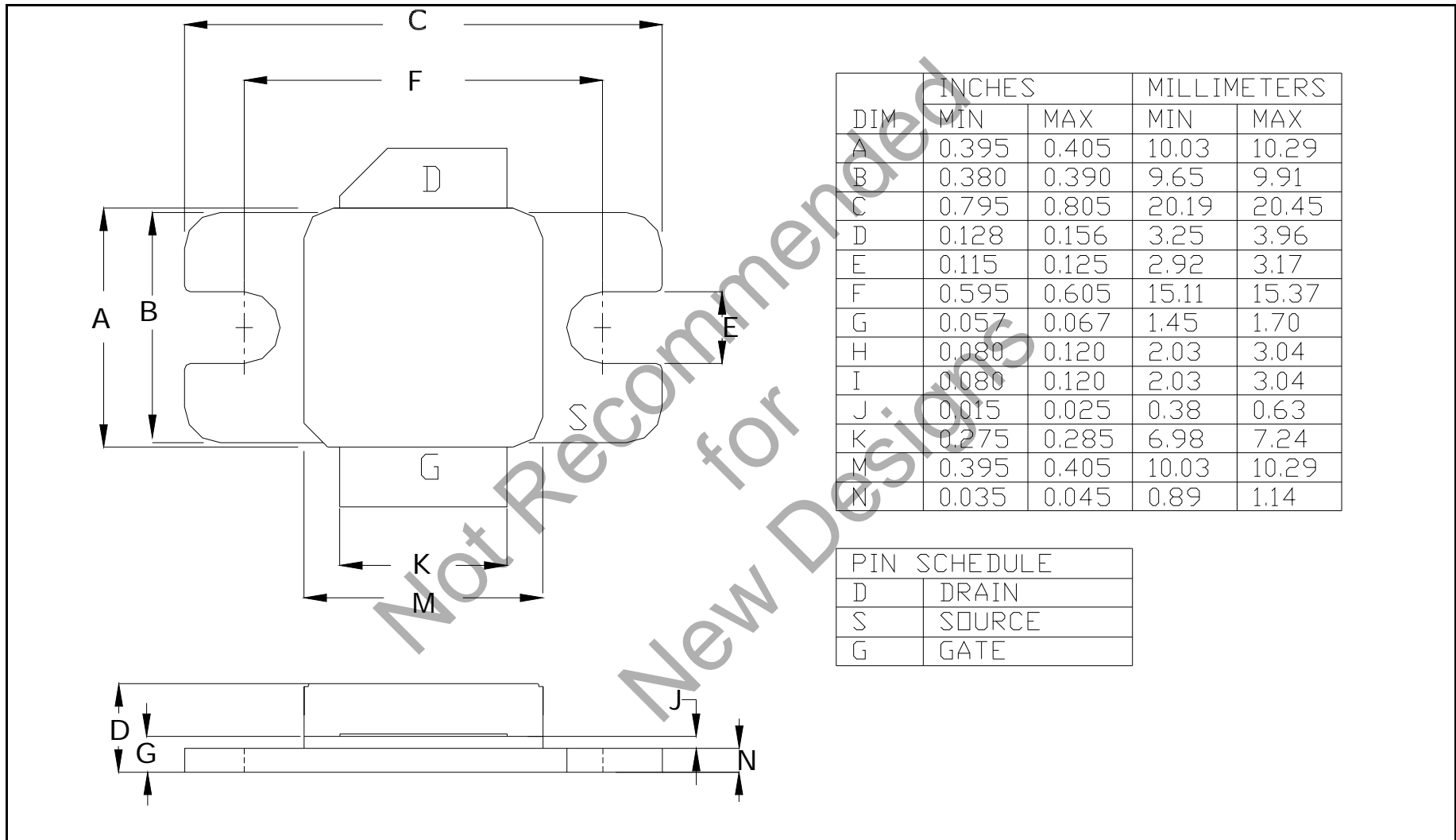
RF TEST FIXTURE IMPEDANCE CHARACTERISTICS

Frequency (MHz)	$Z_{IF} (\Omega)$	$Z_{OF} (\Omega)$
960	2.40 - j0.60	3.67 - j2.42
1090	2.75 - j0.29	3.92 - j1.57
1215	2.83 - j0.32	4.03 - j1.20

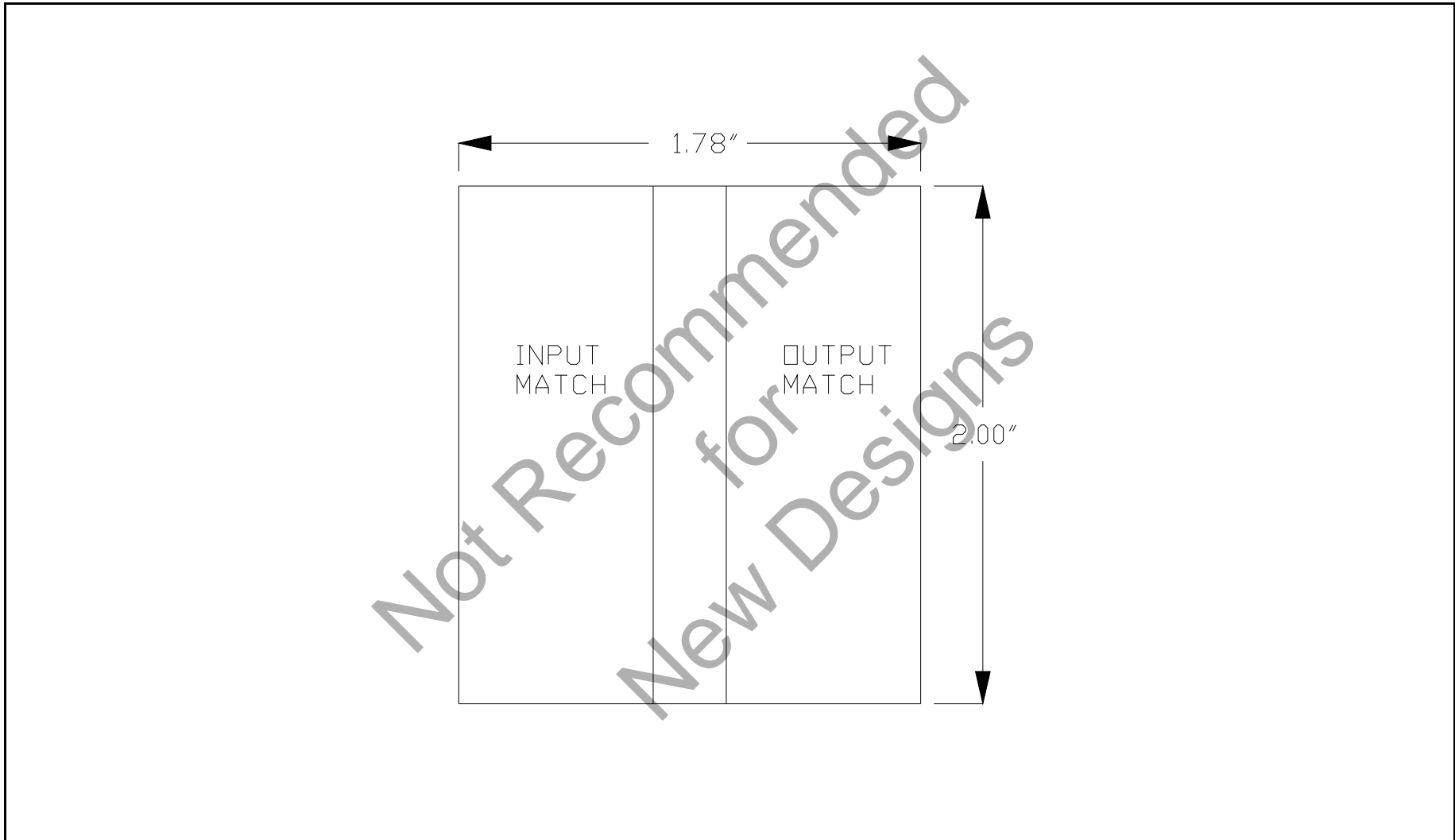
Diagram illustrating the input impedance measurement setup. A 50 Ohm source is connected to the gate (G) of the device through matching circuitry. The drain (D) is connected to a load Z_L . The input impedance is labeled Z_{IN} .

Diagram illustrating the output impedance measurement setup. The gate (G) and drain (D) are connected to matching circuitry. The output impedance is labeled Z_{OUT} .

PACKAGE DIMENSIONAL OUTLINE DRAWING



RF TEST FIXTURE



CONTACT FACTORY FOR RF TEST FIXTURE CAD DRAWING WITH CIRCUIT DIMENSIONS

DEFINITIONS

Data Sheet Status	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
Maximum Ratings	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only. Operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

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Not Recommended for New Designs