

S-Band Radar Miniature Power Amplifier

Part number ILT3035M30 is a miniaturized power amplifier which is internally matched to 50 ohms. It is designed for S-Band radar systems and operates over the instantaneous bandwidth of 3.0-3.5 GHz. It utilizes gold metal LDMOS transistor technology operating in common source configuration. Production RF performance screening is performed at the 100% level while operating under class AB bias ($I_{DQ} = 10\text{mA}$) with a 300us pulse width at 10% duty. The device is operable under a wide range of biasing and pulsing conditions.

50 Ohm Matched

- Requires no external impedance matching circuitry

Silicon LDMOS Transistor

- Gold Metal

Class AB Operation

- Operable under a wide range of bias conditions

Common Source Configuration

- Chip internal Source grounding

Gold Metal System

- Complete Gold System Including Bond-wires
- Maximum Reliability

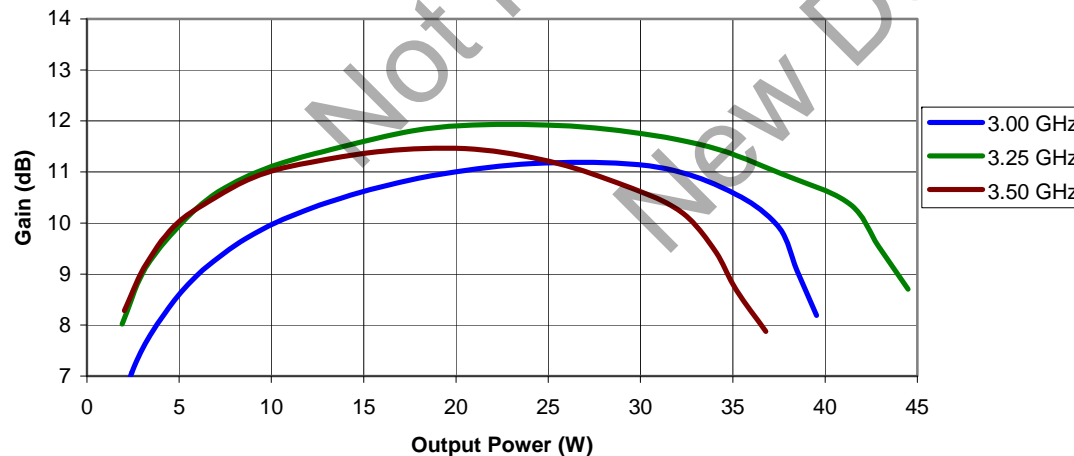
Be0 Free Package

- Metal Based
- Epoxy seal

RF High Power Test

- 100% Device RF High Power Screening

TYPICAL RF GAIN VERSUS OUTPUT POWER PERFORMANCE



MAXIMUM RATINGS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Drain-Source Voltage	V_{DS}	--	65	V	--
BD	Gate-Source Voltage	V_{GS}	-0.5	12	V	--
BD	Storage Temperature Range	T_{STG}	-55	+150	°C	--
BD	Operating Junction Temperature Range	T_J	-55	+200	°C	--
Note	Screen 'BD' = parameter qualified By Design.					

THERMAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	0.6	°C/W	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=TF1, P_{IN}=P_{IN1}, F=F3.$
Note	Screen 'BD' = parameter qualified By Design.					

PROCESSING SPECIFICATIONS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

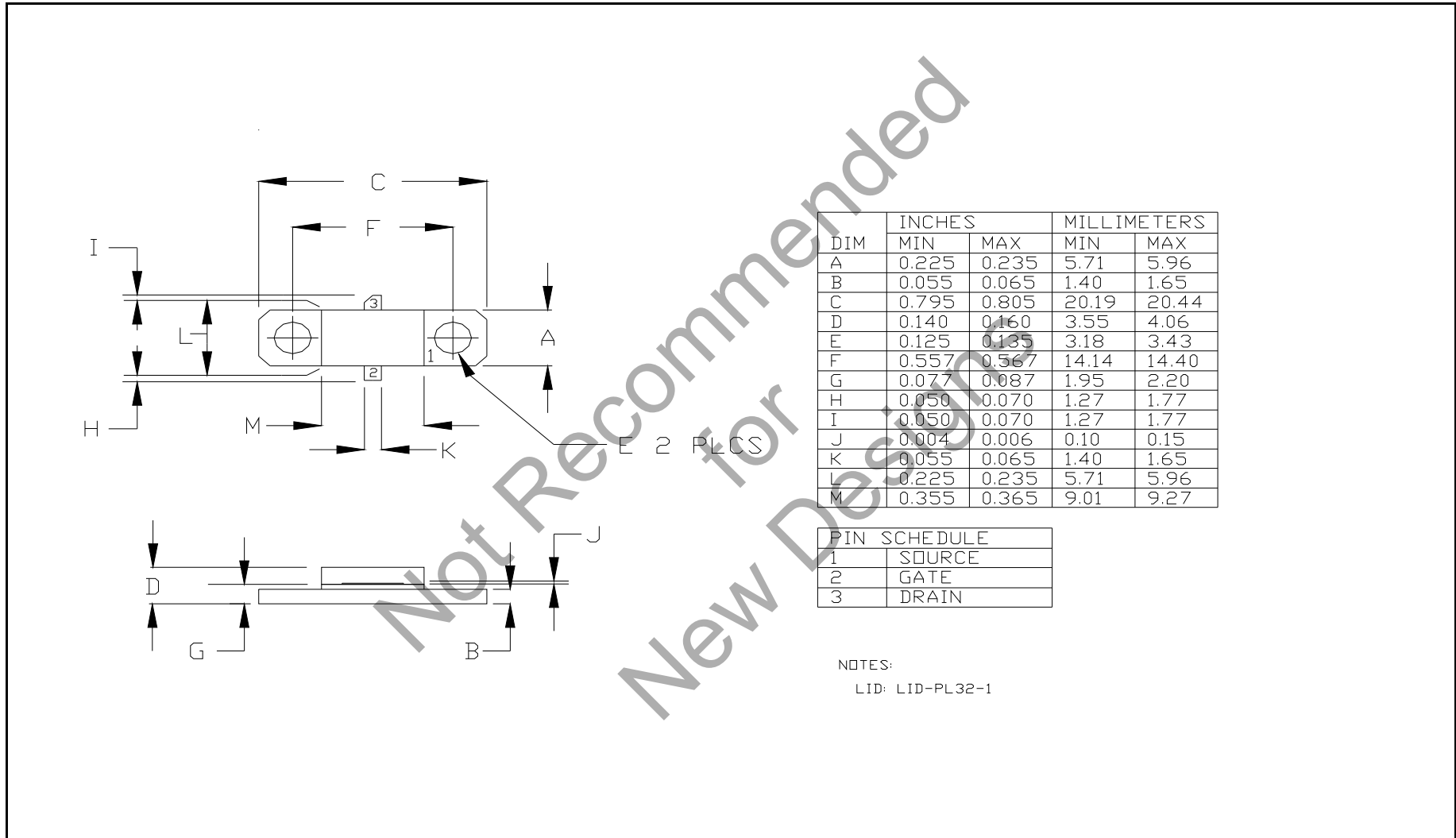
DC ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Drain-Source Breakdown Voltage	BV_{DSS}	65	--	V	$I_{DS} = 10mA, V_{GS} = 0V, T_F = 25\pm5^\circ C.$
100%	Drain Leakage Current	I_{DSS}	--	2.0	μA	$V_{DS} = 32V, V_{GS} = 0V, T_F = 25\pm5^\circ C.$
100%	Operating Gate Voltage	V_{GS}	1.5	4.0	V	$V_{DS} = 5V, I_D = 0.1A, T_F = 25\pm5^\circ C.$
BD	Gate Leakage Current	I_{GSS}	--	2.0	μA	$V_{GS} = 10V, V_{DS} = 0V, T_F = 25\pm5^\circ C.$

RF ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	IRL1	-18	-7	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=TF1,$ $P_{IN}= P_{IN1}, F=F1.$
100%	Input Return Loss	IRL2	-18	-10	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=TF1,$ $P_{IN}= P_{IN2}, F=F2.$
100%	Input Return Loss	IRL3	-18	-10	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=TF1,$ $P_{IN}= P_{IN3}, F=F3.$
100%	Power Gain	G_p	10.0	15.0	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=TF1,$ $P_{IN}= P_{IN1}, P_{IN2}, P_{IN3}, F=F1, F2, F3.$
100%	Power Gain Flatness versus Frequency	GF	0.0	1.3	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=TF1,$ $P_{IN}= P_{IN1}, P_{IN2}, P_{IN3}, F=F1, F2, F3.$
100%	Drain Current - Peak	I_D	1.00	4.00	A	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=TF1,$ $P_{IN}= P_{IN1}, P_{IN2}, P_{IN3}, F=F1, F2, F3.$
100%	Pulse Amplitude Droop	D	-0.50	+0.20	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=TF1,$ $P_{IN}= P_{IN1}, P_{IN2}, P_{IN3}, F=F1, F2, F3.$
100%	Stability into 3:1 VSWR	VSWR-S	--	--	--	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=TF1,$ $P_{IN}= P_{IN1}, P_{IN2}, P_{IN3}, F=F1, F2, F3.$ Rotate 3:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse. All non-harmonically related signals must be at least -65 dBc.
Note 1	$V1 = 32V; I_{DQ1} = 10mA; PW1 = 300\mu s; DF1 = 10\%$					
Note 2	Input Power Test Levels: $P_{IN1} = P_{IN2} = P_{IN3} = 2.0W$					
Note 3	Test Frequencies: $F1 = 3.0 GHz, F2 = 3.3 GHz, F3 = 3.5 GHz.$					
Note 3	$T_F = 25\pm 5^\circ C =$ Device Flange Temperature					

PACKAGE DIMENSIONAL OUTLINE DRAWING

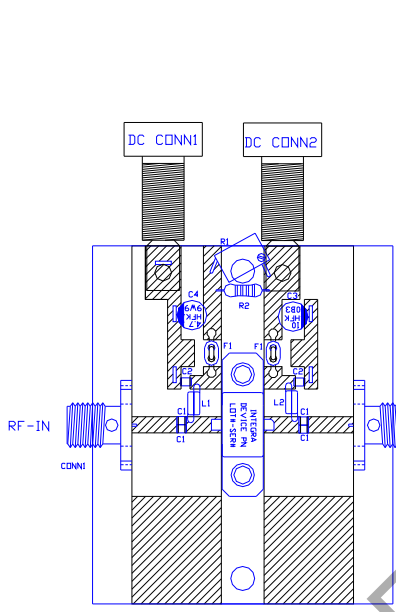


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.225	0.235	5.71	5.96
B	0.055	0.065	1.40	1.65
C	0.795	0.805	20.19	20.44
D	0.140	0.160	3.55	4.06
E	0.125	0.135	3.18	3.43
F	0.557	0.567	14.14	14.40
G	0.077	0.087	1.95	2.20
H	0.050	0.070	1.27	1.77
I	0.050	0.070	1.27	1.77
J	0.004	0.006	0.10	0.15
K	0.055	0.065	1.40	1.65
L	0.225	0.235	5.71	5.96
M	0.355	0.365	9.01	9.27

PIN SCHEDULE	
1	SOURCE
2	GATE
3	DRAIN

NOTES:
LID: LID-PL32-1

RF TEST FIXTURE



The drawing shows a cross-sectional view of the RF test fixture. It features two DC connectors (DC CONN1 and DC CONN2) at the top, two SMA connectors (CONN1 and CONN2) on the sides for RF-IN and RF-OUT, and a central vertical assembly containing various components like capacitors (C1, C2, C3, C4), resistors (R1, R2), coils (L1, L2), and a ferrite core (F1). The central assembly is mounted on a transistor carrier and input/output PC boards, which are supported by a brass carrier and a heatsink.

COMPONENT	DESCRIPTION
DUT	DUT, MOUNT HARD TO THE RIGHT
PC BOARD	ROGERS# 5880, TH=0.031" 1E/1E
C1	CHIP CAPACITOR, TYPE ATC100A, 10 pF
C2	CHIP CAPACITOR, TYPE ATC100A, 20 pF
C3	ELECTROLYTIC CAPACITOR, 10uF / 50V FK DIGI-KEY PN# PCE3808CT-ND, PANASONIC# EEE-FK1H100UR
C4	ELECTROLYTIC CAPACITOR, 4.7uF/50V FK DIGI-KEY PN# PCE3817CT-ND, PANASONIC# EEE-FK1H47R
R1	POTENTIOMETER 1/4" 100kOhms 10%, MOUSER P/N: 652-3266W-1-104LF, MFG P/N: 3266W-1-104LF
R2	AXIAL RESISTOR, 18K OHMS, 1/4W
L1	COIL: 2 TURN AWG# 22 INSULATED, ID 0.0625" DIA, PULL TIGHT AND FULLY CLOSED, LEFT HAND.
L2	COIL: 2 TURN AWG# 22 INSULATED, ID 0.0625" DIA, PULL TIGHT AND FULLY CLOSED, RIGHT HAND.
F1	FERRITE TWIN HOLE CORE, FERRONICS PN# 12-315-J, 1 TURN AWG# 22 INSULATED.
TRANSISTOR CARRIER	2 INCH COPPER - 05
INPUT PC BOARD CARRIER	2 INCH BRASS -01
OUTPUT PC BOARD CARRIER	2 INCH BRASS -01
CLAMP -07 (NOT SHOWN)	INTEGRA DWG: RF TEST FIXTURE HARDWARE NORYL CLAMP W/WINDOW -07
CONN1, CONN2	SMA CONNECTOR, TYPE DS# 2052-5636-02
HEATSINK	2 INCH HEATSINK - 09
DC CONN1	BANANA JACK, BLACK
DC CONN2	BANANA JACK, RED
NOTE	FIXTURE HARDWARE DRAWINGS AVAILABLE ON REQUEST

TOLERANCES UNLESS NOTED			
.X	± .1	X'	± 1"
.XX	± .02	X'X'	± 0'30"
.XXX	± .005		
.XXX	± .0002	FRACTION	± 1/32

MATERIAL: NOTED		Integra TECHNOLOGIES, INC.	
DRAWN: J. BURGER <i>Jill Burger</i>			
CHECKED: J. BURGER <i>Jill Burger</i>	SIZE A	DWG NO. ILT3035M30 RF TEST FIXTURE	REV D
APPROVED: J. DAVIS <i>J. Davis</i>	SCALE: 1:1	SHEET: 1 of 2	

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CONTACT FACTORY FOR RF TEST FIXTURE CAD DRAWING WITH CIRCUIT DIMENSIONS

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DEFINITIONS

Data Sheet Status	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
Maximum Ratings	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only. Operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

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Not Recommended
New Designs