INTEGRA
RF POWER DEVICES

Handling and Adjustment of Integra Technologies LDMOS Evaluation Kits

INTRODUCTION

Integra Technologies loans evaluation kits to customers. Evaluation kits consist of a test fixture with one transistor already mounted inside it together with our test results, plus a spare transistor. For our LDMOS devices then the evaluation kit will either be for an ILDxxxx part which is a transistor that is partially matched within the transistor package to 50Ω or else it will be for an ILTxxxx device which is fully matched to 50Ω within the transistor package.

LDMOS TRANSISTOR HANDLING

LDMOS devices have a Metal Oxide Semiconductor (MOS) gate and hence are very sensitive to ESD damage. Integra does not incorporate any ESD protection diode in its LDMOS devices and so **it is essential that full ESD handling precautions are observed at all times.** ESD precautions must also be observed even when the transistor is already inserted into a test fixture.

LDMOS TRANSISTOR BIASING

LDMOS transistors are enhancement mode devices and so no drain current will flow until a positive voltage is applied to the gate terminal with respect to the source. Since a positive but much higher voltage is also required for .the drain then it is of course possible to operate LDMOS transistors from a single positive supply voltage by incorporating either a potential divider or a voltage regulator for the gate bias. However, Integra LDMOS evaluation kits do not incorporate this extra gate bias circuitry so that the customer can easily vary the gate voltage to examine the effects of different bias points on transistor performance. Consequently, two separate power supplies are required, one for the drain bias and one for the gate bias.

The following sequence should be followed when testing the transistor:

1. Make sure that the RF is turned off before installing the test fixture in the test bench. Make sure that the proper pulse width and duty cycle have been properly set on the RF source prior to turning on the transistor. The transistor may be damaged if the RF source is not set for the correct pulse format.

2. Ensure that the test bench presents good 50Ω source and load impedances to the evaluation kit with, ideally, around 30dB return loss. The output must have a load capable of handling ~3dB more power than both the rated peak output power and the average output power of the transistor.
3. Check the screw torque on the transistor clamp to ensure that the clamp has not loosened during shipment. The screws should be torqued sequentially to between 6-8 in/lbs.
4. The gate bias supply voltage should be adjustable over a range of at least 0V to +5V. Since LDMOS devices have an MOS gate, then in theory no gate current will flow no matter what voltage is applied to the gate within the range specified on the data sheet. This is also true no matter what amplitude of RF signal is applied to the gate up to the maximum value specified on the data sheet. If either the maximum gate voltage or the maximum RF input power is exceeded then it is likely that the gate oxide will be ruptured leading to permanent and irreversible damage to the transistor. In practice, a small gate current will flow due to the finite leakage current of the MOS junction. This current should not exceed the value specified in the data sheet which is typically a few μA maximum.
5. Set the gate supply voltage to 0V. Verify that the voltage on the transistor gate is 0V relative to the heat sink. Measure the resistance between the V_{DD} (RED) and ground (BLACK) terminals. You should measure around 10KΩ through the device drain if the gate supply voltage is properly applied since the channel is turned off.
6. Next connect the charge storage capacitor across the V_{DD} (RED) and GND (Black) terminals. This capacitor usually has a value of 4700μF. This capacitor is needed to minimize pulse droop when the RF signal is applied. After first ensuring that the drain power supply is switched off, connect the drain power supply to the test fixture with the positive output connected to the RED terminal and the GND connected to the BLACK terminal. Set the power supply current limit such that it, in conjunction with the charge storage capacitor, it can handle the maximum peak current expected for the device. Next attach the power supply's voltage sense leads to the V_{DD} and $V_{DD,\ GND}$ terminals if the power supply has this feature available. Ensure that the power supply is in its remote current sense mode. If the power supply does not have a voltage sense capability then connector a voltmeter across the RED and BLACK terminals on the test fixture and manually adjust the drain voltage during RF testing to compensate for any voltage drop.
7. Turn on the $+V_{DD}$ drain power supply and set V_{DD} to the value specified in the data sheet for the transistor. The drain current should not exceed more than a few tens of μA since the gate bias is at 0V to keep the device in pinch off. The current that is flowing is the drain leakage current and its maximum value is specified in the data sheet.
8. SLOWLY increase the gate voltage from 0V until the quiescent current I_{DQ} specified in the transistor's data sheet is achieved. The gate voltage increment should not exceed 50mV to prevent overdriving the gate voltage, thereby inducing excessive drain current and potentially burning out the device. An Agilent E3610A power supply or equivalent is suitable. The gate voltage will typically be around V_{GS} = 3V but may be anywhere in the range 2-5V to achieve the recommended I_{DQ}

value. A spectrum analyzer should be connected at the output to ensure that no oscillations occur as the gate voltage is increased since oscillations can sometimes result in device destruction.

9. Turn on the RF input power starting at a low power (< 0.1W peak), and then increase until the desired output power is achieved. Correlation data is supplied with the clamped device. Please verify correlation with Integra's test results before changing the transistor. The detected RF output pulse should be monitored to ensure that no break up occurs as this may indicate the presence of an oscillation.
9. After the testing is complete turn off the $+V_{DD}$ drain supply voltage first but leave the RF applied for about 5 seconds to discharge the large drain charge storage capacitor. Next, turn off the RF power. Lastly, turn off the gate supply voltage.

DEVICE CORRELATION

The evaluation kit includes the test fixture, an electrolytic capacitor, two transistors, and our RF test data. One of the devices is already clamped into the test fixture. The device has been tested at Integra as installed, and should be used for correlation purposes. Please compare your measured data with Integra's RF data for the serial number installed in the test fixture and reconcile any discrepancies before removing or changing the transistor.

EFFICIENCY MEASUREMENT

Please note that the efficiency recorded in our test data is drain efficiency and not power-added efficiency. At L band there will be only a small difference – about two percentage points - between power added efficiency and drain efficiency since the transistors typically have about 18dB gain. However, at S band the difference is more significant since the gain is in the 10-13dB range resulting in up to five percentage points difference. Please also be aware that the efficiency that is quoted is the efficiency during the pulse and not the efficiency over all time. Integra calculates efficiency from the product of the drain voltage and the average current drawn from the supply divided by the duty cycle. However, the transistor is drawing its quiescent current from the power supply when there is no RF signal applied and this effect is not allowed for in our efficiency data. Consequently, our drain efficiency data underestimates the true efficiency. This effect can be significant, particularly for low duty cycle situations or if a high quiescent current is used (see Reference [1] for a practical example where it is shown that this effect results in the measured efficiency being six percentage points lower than the true value).

TEMPERATURE COMPENSATION

The test fixture does not incorporate thermal compensation of the quiescent drain current. The gate bias voltage may need to be readjusted to maintain a constant I_{DQ} if testing with large variations in ambient temperature.

COOLING

The transistor will dissipate power and requires adequate cooling. As a minimum a biscuit-fan model BT2A1 or equivalent should be provided. This fan can provide 22CFM of airflow over the fins of the heat sink. A #4-40 UNC threaded screw hole is located on the copper carrier underneath the transistor to monitor the flange

temperature. The typical flange temperature for RF testing is 30°C±5°C.

CHANGING THE TRANSISTOR

1. **The transistor is sensitive to ESD, and should be handled and tested in an ESD protected environment.**
2. Thermal grease was used for testing this part. Assuming that the heatsink of the test fixture has been cleaned, then only a small dot of grease 0.03-0.04" in diameter should be applied in the center of the slot. Do not use an excessive amount of grease. The grease pattern after transistor removal should not extend by more than 0.25". The correct amount of grease is required to obtain a thin coat that will not degrade electrical contact. Use Wakefield 120 [2] or equivalent thermal grease.

CONCLUSION

This Application Note has described how to safely use and adjust Integra's LDMOS Evaluation Kits. If additional information is required then please contact Integra Technologies.

REFERENCES

1. Daniel Koyama, Apet Barsegyan, John Walker, "Implications of Using kW-level GaN Transistors in Radar and Avionic Systems", COMCAS Conference, Tel Aviv, Israel, 2-4 Nov, 2015.

2. http://www.wakefield-vette.com/resource-center/downloads/brochures/thermal-management-accessories-wakefield.pdf