A 100W Decade Bandwidth, High-Efficiency GaN Amplifier

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***Abstract*—This paper will report a 100W, 100MHz to 1GHz GaN amplifier module having a minimum efficiency of 48% across the whole band with a minimum gain of 14dB. This is believed to be the highest power/efficiency combination yet reported for this frequency range.**

Keywords—Transistor; GaN; Amplifier; High-Efficiency

1. INTRODUCTION

The design of a high power, high efficiency, multi-octave amplifier with flat gain and low harmonic output is one of the most challenging of all RF design tasks. Krishnamurthy *et al* [1] reported a 100W amplifier at P_{2dB} with 4dB gain ripple covering 100-1000MHz by combining four 25W single-ended transistors. Nagy *et al* [2] have reported an 80W amplifier, also at $P_{2dB,}$ using a single GaN transistor covering 100-1000MHz, but this had 9dB gain ripple across the band. In 2013, Sardin and Popovich [3] reported a decade bandwidth 30W amplifier using a single push-pull GaN transistor but over the much lower 50-500MHz frequency range. In this paper we will report a significant advance with a decade bandwidth amplifier delivering a minimum of 100W at <1dB gain compression over 100-1000MHz using a single push-pull GaN transistor with <3dB gain ripple. Table III compares all these results.

This paper will first consider the appropriate transistor technology for this application, and then discuss the various design architectures that could be used. Finally, the paper will report the results that have been achieved which, we believe, represent a new landmark in terms of power, efficiency and gain flatness across the 100-1000MHz frequency range using just a single transistor.

II. TRANSISTOR TECHNOLOGY

A. GaN vs Si LDMOS

The limit on the maximum output power that can be achieved is determined by the values of the real and imaginary components of the load impedance that the output matching network must present to the transistor. From standard load-line theory [4] the real part of the required impedance at the plane of the current generator in the transistor model is given by $R_L = v_{rf}^2/2P$ where P is the required output power and v_{rf} is the amplitude of the peak drain-source RF voltage. A high value of R_L is needed when trying to match over a multi-octave bandwidth in order to have realizable values for the element values and minimal dissipative loss in the matching network. Consequently, transistors with a high breakdown voltage are used that they can be operated with a high supply voltage such as 50V. GaN, LDMOS, even Si VDMOS satisfy this requirement. However, low capacitance/Watt is also needed, not just because of the Bode-Fano limit on bandwidth matching [5], but also because high output capacitance substantially lowers the required value of load resistance R_L at the terminals of the die from the value given above. GaN on SiC transistors have much lower capacitance/Watt than LDMOS transistors, but this lower capacitance arises because the power density is much higher resulting in increased heat dissipation issues. The GaN devices used in this work are routinely operated at 48V for pulsed applications but can only be operated reliably at 28V in CW mode which reduces the low capacitance/Watt advantage of GaN, and also reduces the value of R_L. Hupfer [6] has achieved 400W across 20-500MHz with a minimum of 55% efficiency and 18dB gain at all frequencies from a single NXP BLF574 LDMOS transistor [7], so it is theoretically possible to achieve a minimum of 100W over 100-1000MHz using a lower power, and hence lower capacitance, LDMOS device. However, GaN was chosen for this work because of its lower capacitance, despite the thermal issues and the need to operate at 28V, because it was believed that higher efficiency would be achieved due to the lower on-resistance.

B. GaN Die Design

Integra manufactures GaN transistor die on a 4" SiC substrate. The gate length is 0.5µm and via holes are not used. The die is designed to ensure low thermal resistance with a two-prong approach: 1) the SiC substrate is thinned down to 3 mil thickness, and 2) the die pitch is 30µm wide which allows heat dissipation through the SiC substrate and also allow enough width for the Au-based source and drain metal fingers for low electro-migration and high long-term reliability. A double field plate design is used together with an extensive gate-drain drift region length for negligible DC-RF dispersion at nominal bias operation.

The double field plate design features a first field plate through a T-shaped gate with 0.5µm gate foot length formed by etching the 1st silicon nitride passivation layer, and a raised gate over-hang on top of the silicon nitride passivation layer. The second field plate is connected to the grounded source

finger inside the active area, and wraps around the gate to reduce feedback (drain-gate) capacitance while at the same time reducing output conductance drain modulation. The combination of the two field plates results in lower electric fields at the surface of the GaN epi-layers and the silicon nitride passivation layer, minimizing trapping and de-trapping effects occurring at the interface. Figure 1 shows an SEM cross-section of the gate and double field plate structure of Integra's 0.5µm GaN HEMT process. A summary of the main processing steps is as follows: Ohmic contacts are made of a Ti/Al/Ni/Au stack followed by an alloying step in RTP. Ion-implantation is used for device isolation. Surface passivation, is accomplished by PECVD low-stress silicon nitride deposition. The gate electrode and gate field plate is formed by a 0.5µm thick Ni/Au metal deposition. Another silicon nitride deposition step is used for isolation between the gate field plate and the source connected field plate, formed next. The second field plate layer is formed with another Au-based metal layer, that also adds metal on top of the source and drain ohmic contacts for lower contact resistance. The final steps of the front-side process include the formation of air bridges and 3µm thick plated Au for the source and drain fingers, as well as the wire bonding pads. Wafer processing is completed after back-grinding the SiC substrate to a 3-mil thickness and another 3µm plated Au back metal deposition. The die is attached to the package flange with an AuSn pre-form at 330 °C.

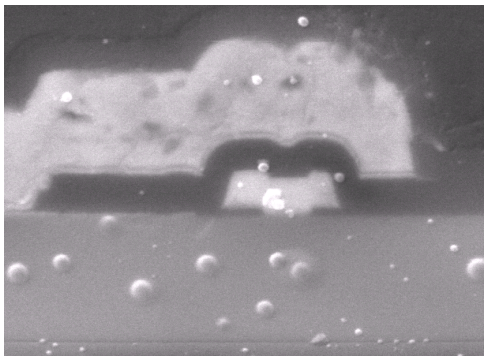

Figure 1. SEM cross-section of Integra's 0.5µm GaN HEMT die with double field plate design.

III. CIRCUIT DESIGN

The requirement for flat gain over a decade bandwidth is most easily satisfied using the distributed amplifier configuration shown in Figure 2. However, distributed amplifiers have severe limitations for high power and high efficiency. At low frequencies the 50Ω load is effectively connected directly across the drain-source terminals of the last die so to achieve 100W requires a 200V peak-peak RF voltage i.e. a breakdown voltage in excess of 200V which, while not impossible for GaN, is not routinely available. It would of course be possible to use a much lower termination resistance for the distributed amplifier and then use a broadband impedance transformer, but its loss would decrease the overall efficiency and the output impedance of the drain artificial transmission line is not purely real rendering the design of such a broadband impedance transformer extremely complex. The use of class A bias is precluded by the need for high efficiency, and because it would exacerbate the thermal issues, so class B bias is needed. However, at low frequencies the harmonics associated with class B will all appear in the load unattenuated, for example in theory the second harmonic will only be 7.4dB below the fundamental. At high frequencies, the low-pass nature of the drain artificial transmission line will prevent the harmonic currents from flowing, thereby degrading the efficiency of the amplifier. Finally, the efficiency of distributed amplifiers is notoriously low because half of the drain current injected into the drain line by each FET flows to the left and half to the right. Techniques such as drain-line tapering can mitigate this effect to some extent but, nevertheless, the efficiency still remains low compared with other circuit topologies.

The *de facto* standard topology for multi-octave high-efficiency amplifiers has always been, and remains so, the class B push-pull amplifier shown in Figure 3, but such amplifiers will exhibit a 6dB/octave gain roll-off which is generally unacceptable. Consequently special techniques are needed to compensate this gain roll-off as discussed below. While higher efficiency has been reported using class E or F, these circuit topologies are incompatible with multi-octave operation since the output matching network is required to present a totally reflecting load to all the harmonics (if it didn't then harmonic energy would be dissipated thereby reducing the efficiency), so the amplifier cannot deliver any power to the load when the input frequency is beyond the first octave. Not only is low harmonic output needed from an efficiency perspective, in many practical applications it is a key system requirement as well. In the case of a push-pull amplifier, low harmonics requires the use of a push-pull transistor with extremely well-matched halves and extreme care in how the center-tapped transformers in Figure 3 are realized in practice.

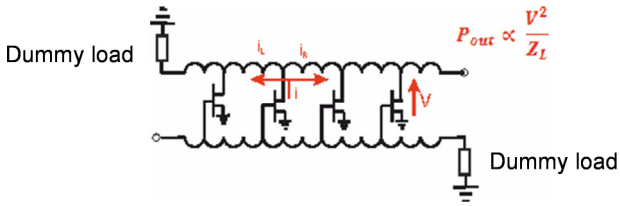

Figure 2. Distributed Amplifier

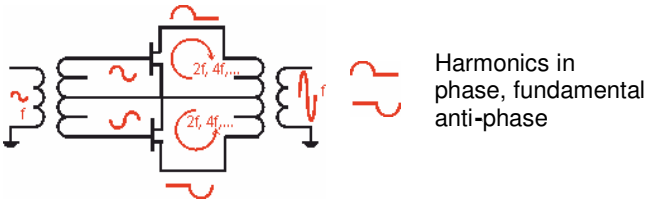

Figure 3. Push-Pull Amplifier

The class B waveform only has even-order harmonics, the push-pull circuit configuration ensures that these cancel in the output center-tapped transformer as they are in anti-phase while the two fundamental drain current components add in phase. The realization of the center-tapped transformer over 100-1000MHz band is key to achieving high efficiency and low harmonics at the output.

IV. 100W 100 - 1000MHz AMPLIFIER

Figures 4 and 5 show, respectively, the circuit diagram of the amplifier and the actual unit. Gate-drain feedback was used together with capacitor-bypassed series gate resistors to achieve flat gain over the bandwidth, and a bias sequencing circuit was incorporated for ease of testing.

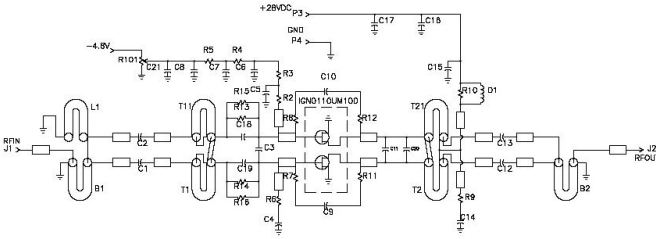

Figure 4. 100-1000MHz Circuit Schematic

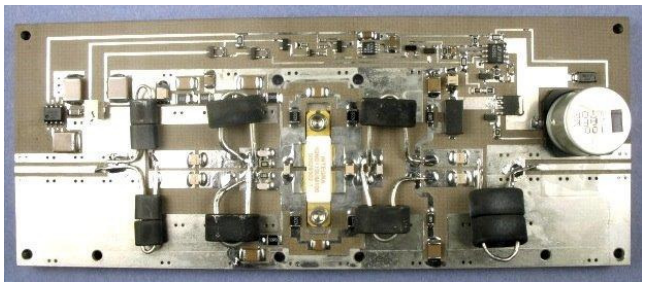

Figure 5. 100-1000MHz 100W amplifier

The transistor was first tested in a load-pull system in order to determine the required source and load impedances for 100W at all frequencies, the results are given in Table I. Even with the low capacitance advantage of GaN, the real part of the optimum load impedance is reduced by an order of magnitude at 1GHz compared with its low frequency value due to the shunting effect of C_{ds}.

Table I. Optimum source and load impedance for 100W (terminal to terminal).

Frequency, GHz	Z_S Ω	Z_L Ω
0.1	10.2 + j0.6	11.3 – j2.7
0.3	13.5 – j1.1	10.8 – j4.7
0.6	8.1 – j6.2	7.8 – j7.2
0.8	6.2 – j4.8	4.3 –j9.2
1.0	6.3 – j12.3	1.3 –j8.3

Aside from needing a transistor with a high supply voltage and low capacitance, the key challenge is the realization of the center-tapped transformers. In this work these were realized by Guanella baluns [8]. It is very important that these are carefully designed in order to achieve as near perfect anti-phase and equal amplitude power split as possible; this is a key requirement for good harmonic cancellation. Coaxial impedance transformers were also used with a 9:1 transformation ratio used at the input and a 4:1 at the output. Each balun and transformer was loaded with ferrite to suppress the unwanted unbalanced current which would otherwise flow at low frequencies and degrade the phase and amplitude split. The inherent 3D nature of the baluns and transformers shown in Figure 5 makes computer optimization of the design parameters (ferrite type, dimensions and position, coaxial lengths and position etc) extremely difficult so considerable experimental optimization was required. For example, it was determined that FERROXCUBE MHB2-13/8/6-4B1 [9] gave the best suppression of low frequency unbalanced currents. Figure 6 shows the effect of two different ferrites on the measured input impedance of the 4:1 transformer when terminated in 12.5Ω load. It can be seen that the ferrite choice has a significant effect on the low frequency VSWR.

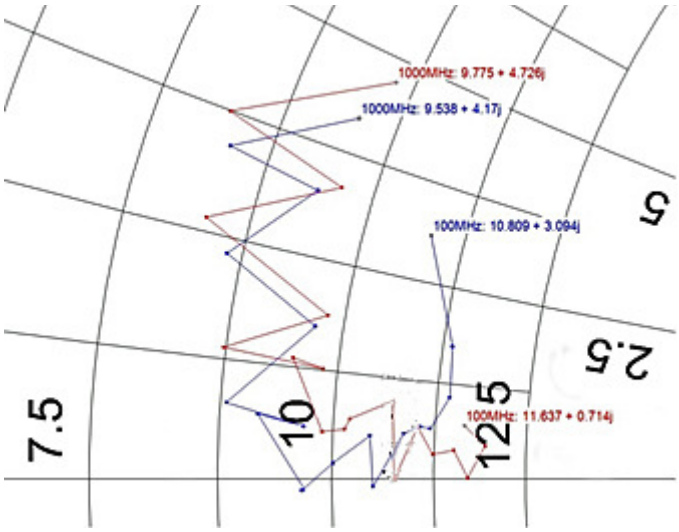

Figure 6. Effect of two different ferrites on 4:1 Impedance Transformer

Figures 7 and 8 show, respectively, the measured gain versus frequency as a function of output power, and the measured efficiency at 100W output. At 100W the amplifier is operating at about 1dB compression at the top of the band and <0.2dB at the low frequency end.

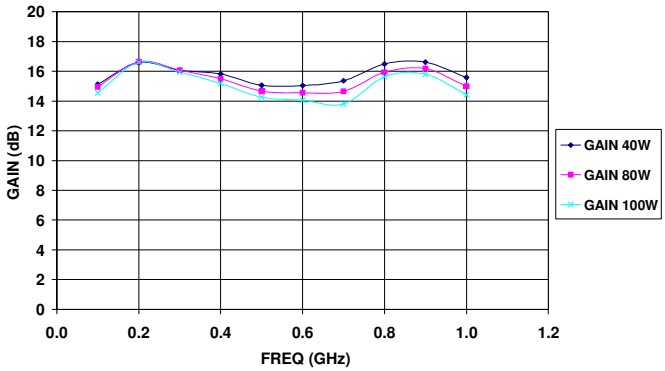

Figure 7. Measured gain versus frequency as a function of output power (V_{ds}=28V, I_{dq}=480mA).

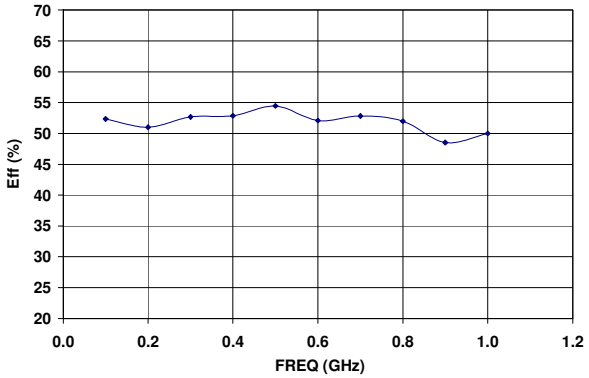

Figure 8. Measured Drain efficiency at 100W output (V_{ds}=28V, I_{dq}=480mA).

Finally, Table II lists the harmonic levels at 100W output. The second harmonic is well suppressed across the entire decade bandwidth with a worst case value of -25dBc, confirming the excellent side-to-side similarity of the two halves of the push-pull transistor as well as the equal-amplitude and anti-phase response of the baluns.

Table II. Second Harmonic Output Levels at 100W output (V_{ds}=28V, I_{dq}=480mA).

Frequency (GHz)	Second Harmonic (dBc)
0.1	-41
0.2	-41
0.3	-40
0.4	-25
0.5	-25
0.6	-30
0.7	-29
0.8	-31
0.9	-44
1.0	-44

V. SUMMARY

This paper has reported a 100W decade bandwidth GaN amplifier with a minimum of 48% efficiency and 14dB gain across 100-1000MHz. This is a significant advance on previous published results as shown in Table III.

Table III. Comparison of this work with previous results

	This work	[1]	[2]	[3]
Transistors	1 PP	4 SE	1 SE	2 SE
Freq (MHz)	100-1000	100-1000	100-1000	50-500
Pout (W)	100	100	80	30
Compression Level (dB)	<1	2	2	**
PAE(%)	48-54	58-72	50-65*	64-83
Gain (dB)	14-17	13-17	13-22	14-16

*Drain Efficiency **Not stated

ACKNOWLEDGMENT

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