Recent Advances in kW-level Pulsed GaN Transistors with Very High Efficiency

James Custer, Gabriele Formicone and John L.B.Walker

Integra Technologies, Inc.
321 Coral Circle
El Segundo
CA 90245
USA
jwalker@integratech.com

Abstract—**This paper reports on GaN transistors having a power output in excess of 1kW for use at L-band frequencies. A 1200W GaN HEMT will be reported with 85% efficiency, this is believed to be the highest power and efficiency combination ever reported for an L band transistor. The importance of using gate pulsing is illustrated to achieve these high efficiencies. The development of GaN transistors that can operate from a 150V drain voltage with a power density of 30W/mm is also reported, and the potential of these new transistors for achieving multi-kW power levels at L band is also considered.**

Index Terms—**Transistor; GaN; Pulsed; High-Power; High-Efficiency**

I. Introduction

Radar systems need a short pulse length in order to detect objects close to the radar (e.g. 6 µs for an object 1 km away), and a low pulse repetition frequency with very high peak power for unambiguous detection of objects far away (e.g. 1.6 kHz prf, equivalent to 1% duty cycle, for an object 100 km distant). These requirements are ideally suited to the characteristics of vacuum tubes such as Magnetrons, Klystrons and Travelling wave Tubes. These devices use kV supply voltages and are capable of supplying MW output power levels at microwave frequencies. Thus a form, fit and function solid-state replacement for a tube-based transmitter needs a transistor with at least 1kW output power in order to make it economically and technically feasible in terms of the number of transistors needed, overall size etc. However, RF power transistors only operate at voltages in the 10's of Volt range which severely limits the peak power that is possible, but they can operate at very long pulse lengths and high duty cycles – even up to CW conditions. This means that by using relatively few transistors with kW power output it is possible to achieve high average power on a par with that from a tube radar so that the overall sensitivity and long range detection performance of the radar is not degraded. However, it is necessary to use pulse-compression technology [1] in order to achieve the same resolution and minimum radar detection range. Thus radar systems designed from the outset to use transistors typically employ pulse lengths in the 100's of µs, up to 20ms even, with duty cycles ≥ 10% and pulse compression ratios of 100 or more. To illustrate the equivalence, a 10 kW peak power solid-state radar that used 50 µs pulse length, 10% duty cycle and 10:1 pulse compression would have the same radar performance in terms of resolution and maximum range as a 100 kW tube radar that used 5 µs pulse length and 1% duty cycle since the mean transmitted power is identical in both cases. It is relatively easy to combine ten 1 kW transistor amplifier modules using a 10-way radial combiner [2]

This paper will first explain why, from a purely technical viewpoint, GaN HEMT transistors are the preferred technology for high power pulsed applications before presenting some examples of state-of-the-art.

II. High-Power Pulsed Transistor Technologies

The first L band pulsed transistors that could supply 1 kW output were Si bipolar. This is a proven and reliable technology that is still in regular production, but it suffers from low gain due to the need to use emitter ballast resistors to prevent thermal runaway, and the need for expensive and environmentally unfriendly BeO packages. No new systems are being designed using Si bipolar transistors. The next technology for this application was LDMOS. This is the cheapest technology, and it is the most robust in terms of VSWR withstand capability. However, it has the lowest efficiency of any of the three technologies due to the use of class A/B bias, and it has an inherent potential failure mechanism due to the presence of the unwanted parasitic bipolar inside the device that can latch-up and cause the transistor to fail if the rise/fall time of the pulse is too fast. As the power of the transistor increases, this problem becomes more acute.

GaN HEMT devices with an RF output power ≥1 kW have only become available within the last year. GaN is a wide band-gap semiconductor which means that the breakdown voltage is much greater than for Si devices, and the 2D electron gas enables a very high drain current density. These two

978-1-5090-2214-4/16/$31.00 ©2016 IEEE

attributes taken together result in a power density of up to 20W/mm of gate periphery – an order of magnitude higher than is possible with Si. However, increased power density is a disadvantage for CW applications due to thermal issues. Only under pulsed conditions can the full benefits of GaN be realized. A consequence of increased power density is a reduced capacitance per Watt, and this not only increases the bandwidth over which 1kW can be achieved, but it also allows the use of harmonic tuning [3] which is required for class E/F operation and the achievement of much higher efficiency than is possible with Si transistors.

III. Examples of State-of-the-Art High-Power Pulsed GaN Transistors

A. *GaN Transistors for Tube Replacements*

As noted in the Introduction, the tube replacement application requires transistors with the highest peak pulse power possible for use under short pulse and low duty cycle. The short pulse and low duty cycle allow the drain voltage to be increased above that which is normally possible for transistors intended for purpose-designed solid-state radars. Figure 1 shows the results achieved by increasing the supply voltage from the normal 50V to 65V for a 1.2-1.4GHz tube replacement amplifier.

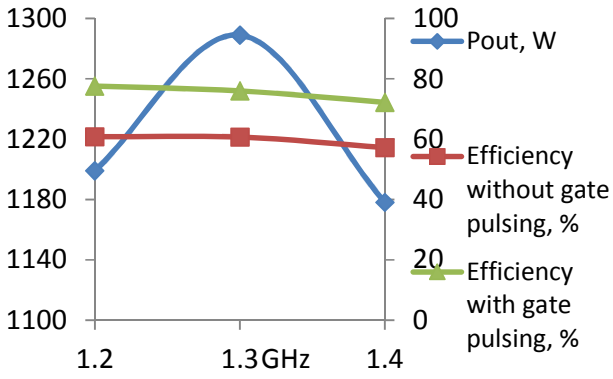

Figure 1. Performance of IGN1214S1000 [4] at 5 µs pulse width, 1.5% duty cycle with V_{dd} = 65V. The input power is 45W.

This transistor delivers more than 1200W across the full radar band with 14dB gain, but the critical thing to note is the substantial efficiency reduction if the transistor bias is not turned off when no RF pulse is applied. GaN transistors, like LDMOS, are operated in class A/B, and the quiescent current required is roughly proportional to the output power. For this particular transistor, the quiescent current is 100mA, but this current flows during the entire pulse off time which, in this case, is 98.5% of the total time. This reduces the maximum efficiency from 75% to just 60%. Another reason why it is important to turn the transistor off when no RF pulse is applied is that the quiescent current generates shot noise which is injected into the receiver via leakage through the T/R switch causing receiver desensitization.

Ideally, the drain current would be switched to ensure that the drain current is reduced to zero in the off period, but this requires switching 18A of drain current which is a non-trivial issue. A simpler solution is to switch the gate voltage, but there will still be some residual drain current in this case due to the finite drain-source leakage current that causes a small amount of receiver desensitization. Nevertheless, over 30dB noise suppression is achieved using gate switching in a practical situation [5].

B. *GaN Transistors for IFF and SSR Applications*

Identify Friend or Foe (IFF) and Secondary Surveillance Radar (SSR) systems send out an interrogating pulse train at 1030MHz and the transponder on board the aircraft sends back a reply at 1090MHz. The ground based transmitter is normally required to have a 4 kW output power while the transponder is normally in the 1-2 kW range. 1kW transistors are ideal for these systems since it is easy to combine 4 in parallel for the ground-based transmitter and two for the airborne one. However, the four-way combiner has some loss and so a power level >1200W from the transistor is preferred. The two most common pulse trains are either standard Mode S or Extended Length Message Mode S which is commonly referred to as Mode S ELM. Mode S ELM is the more technically demanding of the two pulse trains and consists of a burst of 48 pulses of 32 µs on, 18 µs off (i.e. 67% duty cycle within the pulse burst) with a long-term duty cycle of 6.4%. From a thermal perspective this looks like a 2.4ms pulse at 6.4% duty cycle. Figure 2 shows the performance of a 1200W GaN transistor for this application which operates at both 1030 and 1090 MHz.

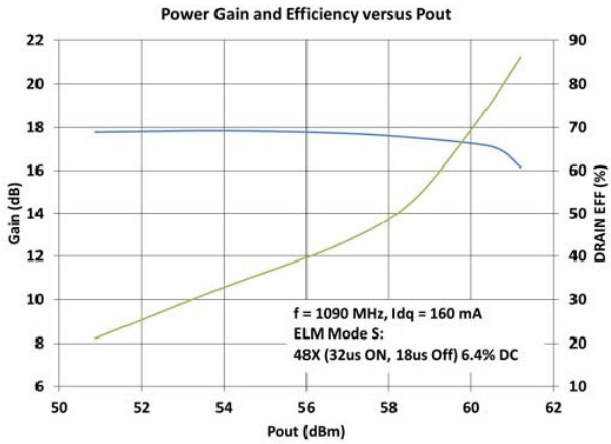

Figure 2. Performance of IGN1011L1200 [6]. V_{ds} = 50V.

Efficiencies in the 90% range have previously been reported using class E or F mode operation, but these results have invariably been obtained at relatively low output power in the 10-100W range, e.g. 93.6% at 26.8W using class E [7]. 1200W with 85% efficiency is believed to be the highest power and efficiency combination yet reported for a GaN transistor. The key to achieving this efficiency is the use of harmonic tuning in the output matching circuit. This example demonstrates that the output capacitance of even a very large GaN transistor is still sufficiently low that the harmonics are not totally shorted within the device so that harmonic tuning is possible. This

is a key advantage of GaN compared with LDMOS. The typical efficiency of a 1kW LDMOS device for this application is 55%, 30% less than is achieved with GaN. The large C_{ds} of LDMOS prevents any harmonic tuning. The efficiency reported in Figure 2 is the efficiency within the pulse, the effect of quiescent current in the off period has been gated out. The higher duty cycle of 6.4% reduces the effect of quiescent current in the pulse off period compared with the previous 1.5% case but, nevertheless, the effect is still significant unless gate pulsing is used due to the higher quiescent current (160mA compared with 100mA).

Table 1 lists the impedances that the circuit must present to the transistor in order to achieve the performance given in Figure 2. Also shown in Table 1 are the corresponding impedances required for an LDMOS 1030 MHz, 950 W transistor. It can be seen that the impedances at the output are about a factor of two higher for the GaN transistor even though this is a higher power transistor. V_{ds} = 50V in both cases. Neither transistor incorporates any matching inside the package at the output of the device. The higher impedance is a direct consequence of the reduced output capacitance C_{ds} of the GaN device compared with LDMOS. This can be seen from a simple analysis as shown in Figure 3.

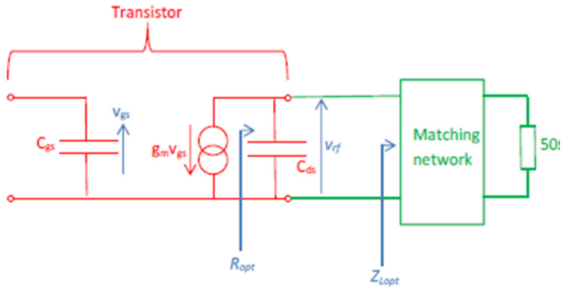

Figure 3. Load-Line Analysis.

From standard load-line analysis, $R_{opt} = V_{rf}^2/2P$ and so R_{opt} = 1.25Ω if V_{ds} =50V for P = 1kW, assuming 100% voltage modulation. Analysis of the circuit in Figure 3 shows that the optimum load impedance at the output of the die is given by:

$$Z_{Lopt} = \frac{R_{opt}}{1 - j\omega C_{ds} R_{opt}} \quad (1)$$

The real part of Z_{Lopt} is given by:

$$\text{Re } Z_{L,opt} = R_{opt}/(1+(\omega C_{ds} R_{opt})^2) \quad (2)$$

Using the data in Table 1, it can be deduced from Equation 2 that C_{ds} for the GaN transistor is 99pF while it is 232pF for the LDMOS device even though the GaN transistor has 26% higher output power.

Transistor	$Z_{S,\,opt}$ F_0 Ω	$Z_{L,\,opt}$ F_0 Ω	$Z_{L,\,opt}$ $2F_0$ Ω
IGN1011L1200	1.9-j1.7	0.9+j0.15	0.4 +j5.6
ILD1011L950HV	0.4+j0	0.4+j0.8	

Table 1. Optimum source and load impedances at the package reference plane for IGN1011L1200 (GaN 1200W) and ILD1011L950HV (LDMOS 950W). V_{ds}=50V in both cases, Mode S ELM operation.

Finally, Figure 4 shows photos of the GaN and LDMOS devices, it can be seen that the GaN device is also physically smaller. Although it may appear that the LDMOS part is push-pull, in operation the two input and two output terminals are shorted together on the PCB so that the device is operated single-ended.

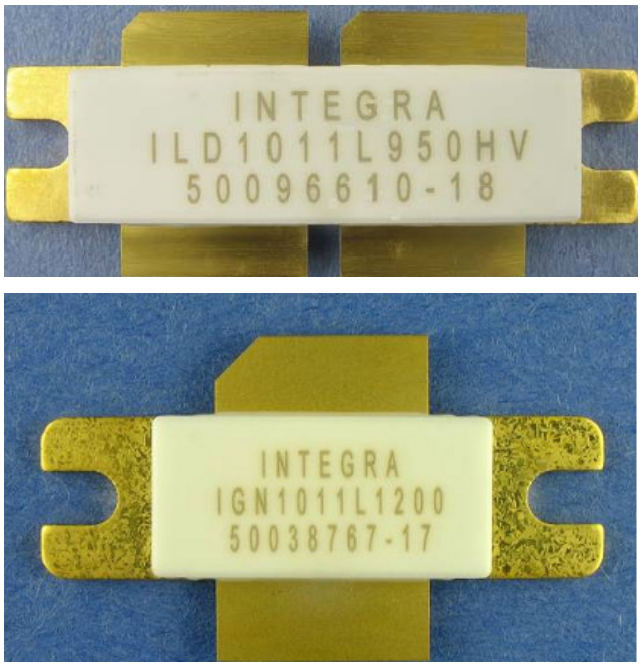

Figure 4. Photographs of GaN (bottom) and LDMOS (top) 1030 MHz Transistors.

C. *High Voltage GaN transistors for RF and Microwave Applications*

The drain supply voltage for most high-power pulsed GaN transistors for use at RF and microwave frequencies is 50V or less, with the notable exception of the tube replacement device mentioned previously. There are basically only two ways to increase the RF output power, either the current needs to be increased which equates to increasing the number or size of the die in the package, or else the supply

voltage needs to be increased. Increasing either the number or size of the die adds directly to the cost of the transistor, and there is only limited scope for doing this since there are limits to the size of package available, and the existing 1kW devices almost entirely fill the available space inside the package already. The better solution is to increase the supply voltage since this has no impact on cost and it maintains the required load impedance at a high value.

GaN transistors have been developed that operate from a drain bias up to V_{ds} = 150V by increasing the Fe concentration in the buffer layer [8]. Figure 5 shows the measured RF performance from a single die of one of these devices at V_{ds}=150 V under 100 µs, 10% duty cycle pulse conditions. The test frequency in the case was 430MHz. Since the gain at 430MHz is 27dB, then with 6dB/octave gain roll-off it can be assumed that the gain at 1030MHz would be around 20dB. The total gate periphery is 15mm giving an almost record power density of 30W/mm. Figure 6 shows a photograph of the device. The GaN die occupies about one-third of the total die attach length, and since the die attach length is a little over half that of the package used for the 1200 W part shown in Figure 4, then by extrapolation it is easy to see that if enough of these high voltage die were inserted into the same package as used in Figure 4 then it would be possible to produce a single transistor with an output power in the 2-3kW range. This would lead to substantial cost and size reductions of the equipment that it was used in.

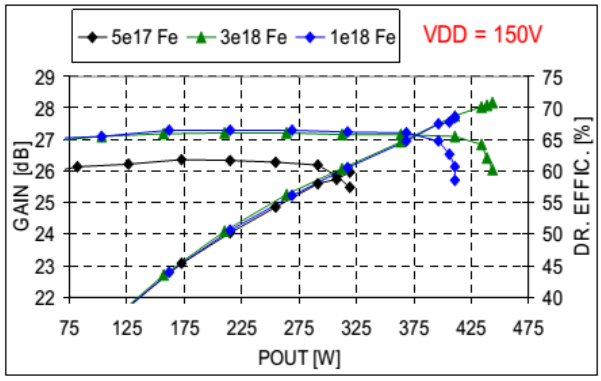

Figure 5. RF performance at 430MHz under 100 µs, 10% duty cycle of a single high voltage GaN die as a function of Fe concentration.

Of course, the obvious question which immediately arises from a die operated at such a high power density of 30W/mm is whether it is reliable? Extensive thermal modelling has been performed to determine the peak junction temperature. The simulations were performed at Vds = 125V, Pout =350W, 100 µs, 10% pulse conditions. The measured drain efficiency in this case was 76% giving a total power dissipation within the device of 110W. The calculated peak junction temperature under these conditions with a case temperature of 26 ^{0}C is only 72 ^{0}C leading to a pulsed thermal resistance of 0.42 ^{0}C/W. It is thus concluded that there is no issue with reliability as far as thermal issues are concerned.

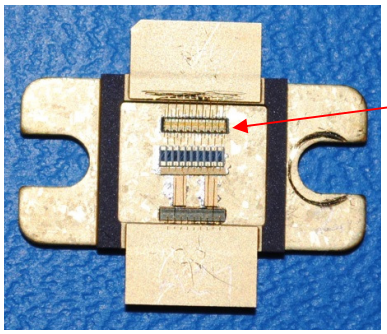

Figure 6. Photograph of the transistor used for the data in Figure 5.

IV. SUMMARY

This paper has reported recent results obtained on very high-power pulsed GaN transistors developed for use at L band. A 1200W 1030MHz device has been reported with an efficiency of 85%; this is believed to be the highest power and efficiency combination yet reported for a GaN transistor. New high voltage GaN transistors have been described that operate from drain voltages as high as 150V with 30W/mm power density. It has been shown that it should be possible to produce GaN transistors using these high voltage die with an output power in the 2-3kW range.

REFERENCES

[1] J.R. Klauder, A.C. Price, S. Darlington and W.J. Albersheim, The Theory and Design of Chirp Radars", Bell System Technical Journal, Vol. 39, pp. 745-809, July 1960.

[2] G.W.Swift and D.I.Stones, "A Comprehensive Design Technique for the Radial Wave Power Combiner", IEEE MTT-S Symposium, pp.279-281, 1988.

[3] P. Colantonio, F. Giannini, E. Limiti, G. Leuzzi, "Input/Output Optimum 2nd Harmonic Terminations in Low Voltage High Efficiency Power Amplifiers", Proceed. of 10th Microcoll, Budapest, March 1999, pp. 401-405.

[4] http://www.integratech.com/ProductDoc.ashx?Id=1240.

[5] D.Koyama, A. Barsegyan and J.Walker, "Implications of Using kW-level GaN Transistors in Radar and Avionic Systems", IEEE COMCAS Conference, Nov 2-4, 2015.

[6] http://www.integratech.com/ProductDoc.ashx?Id=1251.

[7] W. Chen, R. A. Chinga, S. Yoshida, J. Lin, C. Chen, and W. Lo, "A 25.6 W 13.56 MHz wireless power transfer system with a 94% efficiency GaN Class-E power amplifier," in IEEE MTT-S Int. Microwave Symp. Dig., June 17–22, 2012, pp. 1–3.

[8] G. Formicone and J.Custer, "Analysis of a GaN/SiC UHF Radar Amplifier for Operation at 125V Bias" , 10th European Microwave Integrated Circuits Conference, pp.192-5, 2015