INTEGRA
RF POWER DEVICES

Automatic & Fail-Safe Biasing of GaN Transistors

INTRODUCTION

GaN HEMT transistors are depletion mode devices and so require a negative voltage for the gate and a positive voltage for the drain. It is sometimes inconvenient to have to provide both positive and negative supply voltages. Also, since they are depletion mode devices IT IS CRITICALLY IMPORTANT TO SUPPLY A NEGATIVE VOLTAGE TO THE GATE BEFORE ANY POSITIVE VOLTAGE IS APPLIED TO THE DRAIN as otherwise the transistor will draw its maximum possible drain current from the supply which is likely to lead to excessive thermal dissipation and the device burning out. For these reasons Integra Technologies has developed a fully automatic and fail-safe bias circuit for its GaN transistors that only requires a single positive voltage power supply.

CIRCUIT OPERATION

Figure 1 shows a block diagram of the circuit while Figure 2 shows the circuit in complete detail. A diode detector connected to a coupler is used to sense when an RF signal is applied to the transistor. There are two stages of operation of this circuit. In the initial phase,

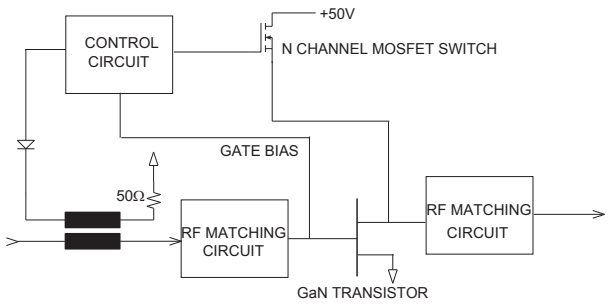

FIGURE 1: Block Diagram

which will be described first, a negative voltage is applied to the gate of the GaN transistor such that when the drain bias is subsequently applied then the device will be biased at pinch-off i.e. no drain current will flow save for the finite leakage current of the transistor as specified in the transistor's data sheet. This bias sequence of first applying a negative gate voltage followed by the application of the positive drain bias is fail-safe and fully automatic, and is controlled by the circuit. Integra refers to this circuit as a **G**ate **P**ulsing and **S**equencing circuit (**GPS** circuit), and this first phase of operation is the sequencing aspect.

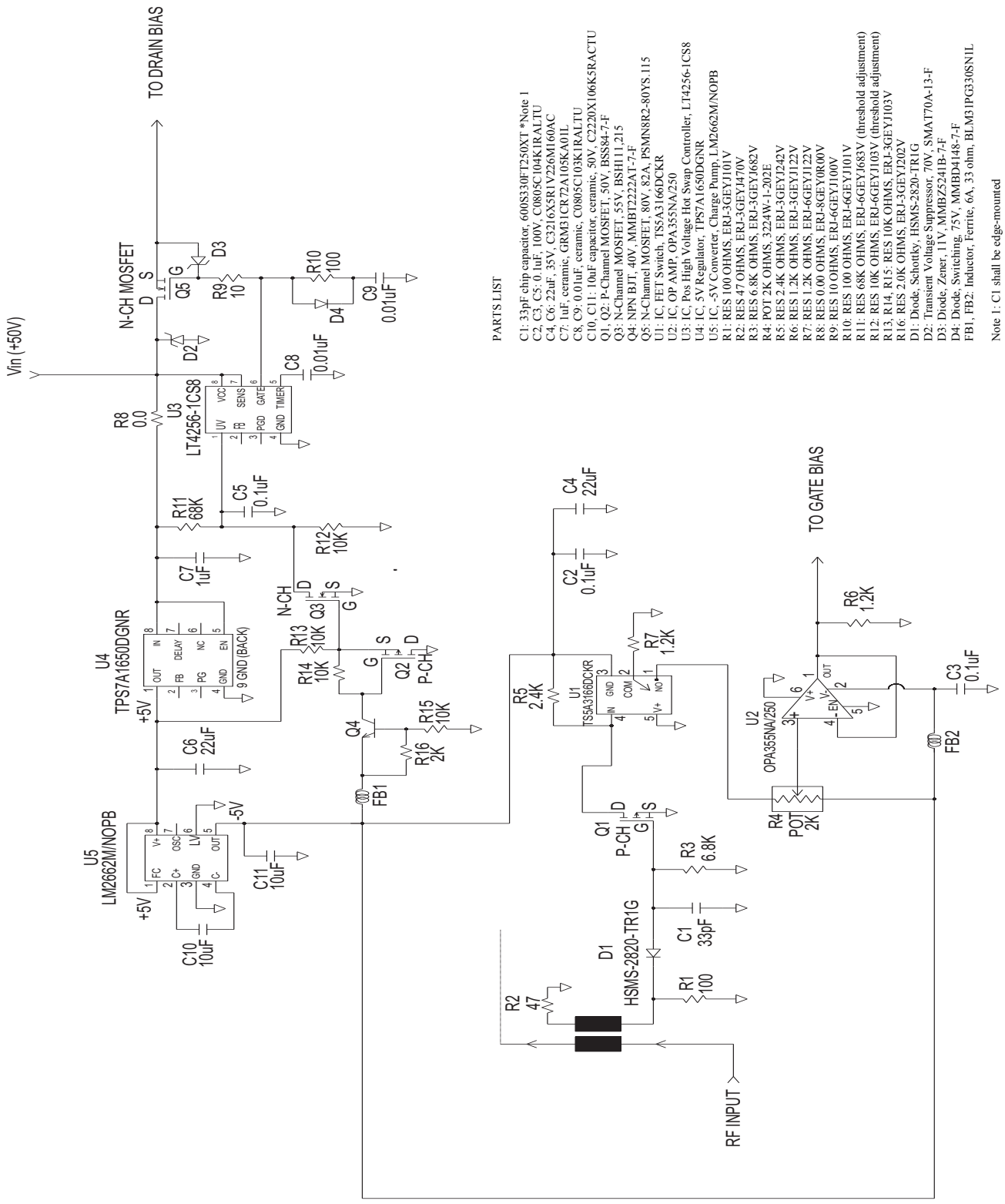

FIGURE 2: GPS Circuit

In the second phase of operation, when the diode detects the presence of an applied RF pulse then the circuit sets the gate bias voltage to the value required to achieve the desired quiescent current I_{DQ} after which the transistor amplifies the RF signal. In the off period of the RF signal the gate voltage returns once more to the pinch-off voltage. This is the gate pulsing aspect of the circuit.

There are four important points to note about using this GPS circuit. The first is that there is obviously a finite delay between the application of an RF pulse at the input and the GaN device turning on, and likewise for the turn off sequence., and these delays and the associated rise and fall times are detailed later on in this application note. The second point is that this circuit has a very beneficial effect on reducing the amount of shot noise injected into the receiver during the RF-off period. Silicon bipolar RF power transistors are operated in class C and have the exceedingly desirable feature of automatically ensuring that no DC current flows through the transistor when there is no applied RF signal to the input of the transistor. This ensures that there is no receiver desensitization due to shot noise being injected into the receiver from any DC quiescent current flowing through the transistor in the RF-off period. However, GaN HEMT and LDMOS devices are always operated in class A/B and so without setting the gate voltage to its pinch-off value in the RF-off period then these transistors will pass their normal quiescent current which will inject shot noise into the receiver and cause desensitization. The GPS circuit automatically sets the gate voltage to its pinch-off value in the RF-off period and so almost eliminates shot noise injection. A small residual drain current will still flow even when the gate voltage is set to its pinch-off value due to the transistor's finite leakage current, but the effect is greatly reduced, and an example of the amount of improvement in receiver sensitivity is given later on.

The third advantage of using this GPS circuit is that the overall system efficiency is improved since there will be no power dissipated in the transistor, except that caused by the finite leakage current, in the RF-off period. This effect can be quite significant since many radar systems operate at 10% duty cycle or less, i.e. the transistor is dissipating the product of its supply voltage and quiescent current for 90% of the time. Eliminating DC power dissipation in the RF-off period can increase the overall system efficiency by six percentage points [1]. However, there will be a very small reduction in efficiency during the pulse, typically 0.3%, due to the finite voltage drop of about 0.2V across the ultra-low $R_{DS,on}$ MOSFET used as the drain switch for the GaN transistor.

The final advantage of using this circuit is that the user only needs to supply a single positive voltage to the test fixture, all other voltages are generated internally.

The detailed operation of this circuit is as follows: Referring to the schematic in Figure 2, an N-channel power MOSFET Q5 is used as a drain switch connecting the positive supply to the drain of the GaN device. Q5 has a very low $R_{DS,on}$ of 8.5 mΩ to minimize the voltage drop, and it can pass up to 80A of drain current which is adequate for all of Integra's GaN transistors. Q5 is switched on and off via the gate pin (pin 6) of controller U3. At initial DC power-up, transistor Q5 remains off while the +5V voltage regulator U4 and voltage inverter U5 turn on. The output of U4 drives the input of U5 to

produce the -5V needed for the GaN transistor gate biasing. When the positive supply voltage reaches about +4V, U5 begins to turn on and a negative voltage appears at its output. When the output voltage of U5 reaches about -4V, NPN transistor Q4 turns on, which then turns on the P-channel MOSFET Q2. With Q2 on, its source terminal goes to 0V, turning off the N channel MOSFET Q3. The open-circuit at the drain of Q3 disconnects it from the UV pin (pin1) of U3 and allows normal operation of the controller U3 to proceed. Whenever U5 is off or not fully on i.e., when its output is -4V or less then Q3 will be on, pulling the UV pin of the controller U3 down to 0V and forcing U3 to turn off Q5. This ensures that no drain voltage is applied to the GaN device when the voltage inverter output is not at least < -4V, and that the GaN device will always be pinched off initially when drain voltage is being applied to it.

As power-up proceeds, U3 becomes active and assumes control of the remaining bias sequencing process. When the UV pin of U3 reaches the low-to-high threshold voltage of 4V, the gate pin (pin 6) of U3 begins to turn on Q5 allowing drain voltage to be applied to the GaN device. The supply voltage at which this occurs is determined by the voltage divider action of resistors R11 and R12:

$$V_{Supply} = 4V\ x\ \frac{R11 + R12}{R11} \qquad (1)$$

As an example, for R11=68K and R12=10K, then the drain will begin to turn on when V_{Supply} reaches 31V. The gate pin of U3 utilizes a charge pump to provide a linear ramp-up of the drain voltage. This ramp-up time can be adjusted with capacitor C9.

For power-down, the process occurs in reverse except that the threshold level is slightly offset due to the built-in hysteresis in the controller U3 (high-to-low threshold is 3.6V for UV pin). For the example given above, the high-to-low threshold can be determined by replacing 4V with 3.6V in equation (1) whence Q5 turns off when the supply voltage crosses 28V.

All that has been described so far is the safe application of drain voltage to the GaN device. Up to this point, the GaN transistor does not pass any drain current, except for a small finite leakage current whose maximum value is specified in the transistor's data sheet, since the -5V output from the voltage regulator U5 is applied via the operational amplifier U2 to the gate of the GaN transistor which causes pinch-off. The gate pulsing circuit is DC-powered from the -5V output of the voltage inverter U5, but otherwise operates separately from the drain bias sequencer. When an RF pulse is applied, a Schottky diode detector D1 triggers the comparator/switch U1 which switches the gate voltage to the desired operating bias level. The gate bias voltage is determined by the potentiometer R4. For fast switching time, a high-speed rail-to-rail op-amp was used in the buffer amplifier. Also, capacitance on the gate bias line following the switch was minimized to maintain a fast rise/fall time. The total power consumption of this gate pulsing and sequencing circuit is 0.85W (17mA at 50V). In the RF-off period the GaN transistor is once more biased at pinch-off so that there is no power dissipation in the transistor in the off-period except for that caused by the finite leakage current.

The above has been a description of full automatic and fail-safe biasing of GaN transistors using a diode to detect

The above has been a description of full automatic and fail-safe biasing of GaN transistors using a diode to detect the presence of an RF pulse. However, there may be situations where the use of a quarter-wave coupler and diode detector is either unwanted or impractical for size reasons. It is of course possible to omit the coupler and detector circuit and turn on the gate bias by inserting a voltage divider and switch connected between the -5V output of U5 and ground, and connecting the mid-point of the divider to the gate of Q1. However, this will result in quiescent current flowing in the RF-off period with the consequent reduction in system efficiency as well as the injection of shot noise into the receiver.

TIME DELAY & RISE/FALL TIME MEASUREMENTS

Figures 3 and 4 show the RF output pulse waveform with and without gate pulsing, respectively, from which it can be seen that the rise and fall times with (without) gate pulsing are 100ns (59ns) and 16 ns (15ns), respectively. Also, it is obvious that there must also be a delay between the application of the RF pulse and the pulse at the load, this delay is shown in Figure 5 and is typically 10ns.

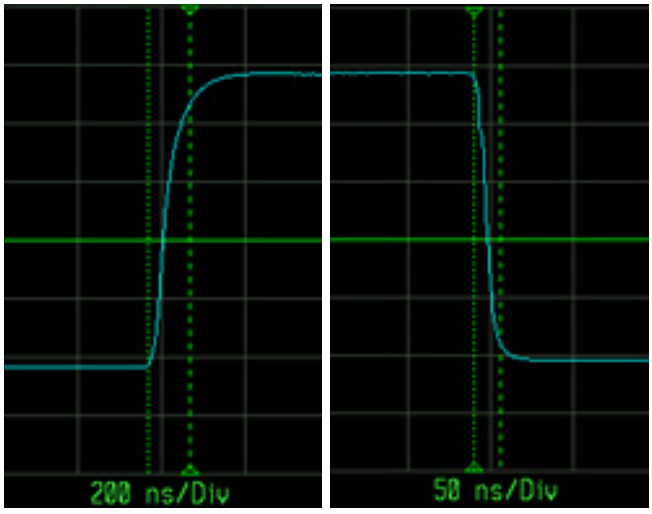

FIGURE 3: RF output Waveform with Gate Pulsing

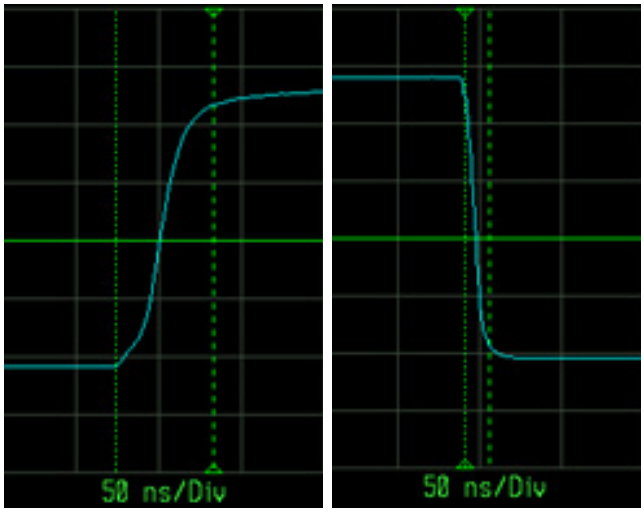

FIGURE 4: RF output Waveform without Gate Pulsing

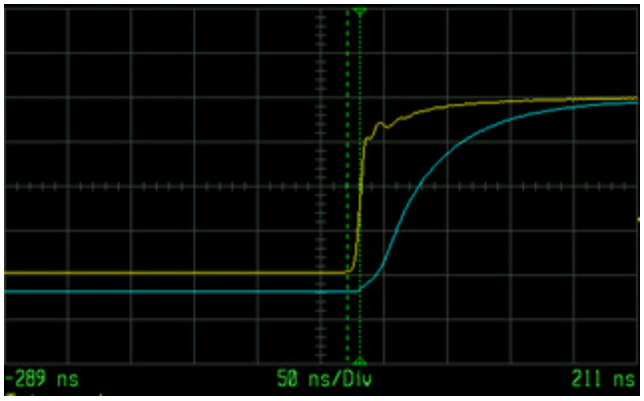

FIGURE 5: Time Delay between RF Input and Output Pulses

NOISE SUPPRESSION

Of critical importance is the determination of the output noise improvement in the pulse-off period as a result of using the gate pulsing and sequencing circuit. This data is given in Table 1 from which it can be seen that >30dB suppression was achieved. This data was obtained using a 500W transistor that used 200mA quiescent current in normal operation.

Frequency GHz	Input Noise dBm/Hz	Output Noise Normal Gate Bias dBm/Hz	Output Noise Gate Pulsing dBm/Hz
1.2	-126	-113	-147
1.3	-126	-113	-147
1.4	-126	-113	-148

TABLE 1: Amplifier Noise Power: normal gate bias vs. gate pulsing for I_{DQ} = 200mA.

TEMPERATURE COMPENSATION

If a constant gate voltage is applied to a GaN transistor then the quiescent current will decrease as the temperature is increased. If a constant quiescent current is desired over temperature then it is necessary to incorporate a temperature compensation circuit. A typical implementation is shown in Figure 6, where the temperature-dependent base-emitter voltage of PNP transistor MMBT2907 is used to generate the compensating voltage. Figure 7 shows I_{DQ} vs. temperature and Figure 8 shows gate voltage vs. temperature (for constant Id_{DQ}) for Integra GaN transistor IGN1214M500 .Approximately +0.6 mV/°C gate voltage compensation is required for this transistor.

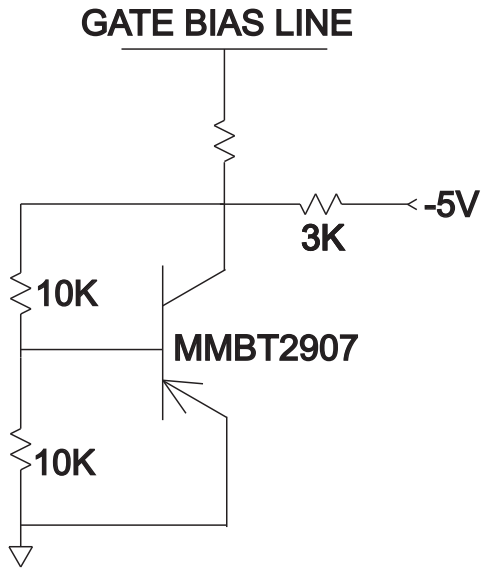

FIGURE 6: Temperature Compensation Circuit

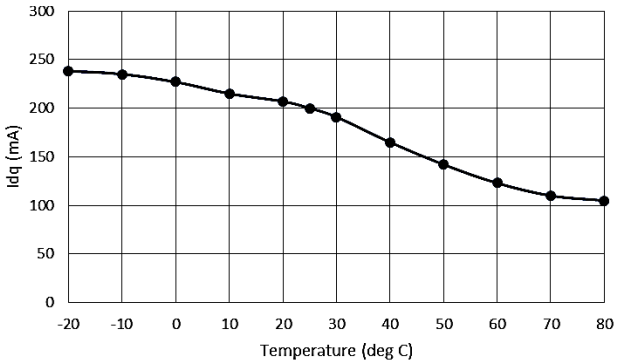

FIGURE 7: I_{DQ} vs. Temperature.

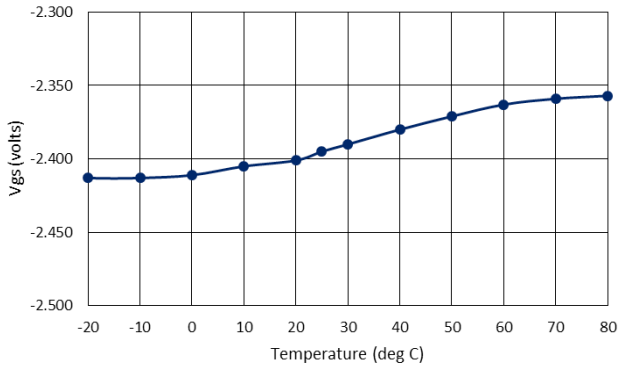

FIGURE 8: V_{GS} vs. Temperature for Constant I_{DQ}.

CONCLUSIONS

This application note has described a circuit for fully automatic and fail-safe biasing of GaN transistors. Time delay and rise/fall time measurements have been presented. Finally, it has been shown that the circuit suppresses the output noise in the RF-off period by >30dB for a 500W GaN transistor biased with a quiescent current of 200mA.

REFERENCES

1. Daniel Koyama, Apet Barsegyan, John Walker, *"Implications of Using kW-level GaN Transistors in Radar and Avionic Systems"*, IEEE COMCAS Conference, Tel Aviv, Israel, 2-4 Nov. 2015.