INTEGRA
RF POWER DEVICES

Handling and Adjustment of Integra Technologies GaN-on-SiC HEMT Evaluation Kits

INTRODUCTION

Integra Technologies loans evaluation kits to customers. Evaluation kits consist of a test fixture with one transistor already mounted inside it together with our test results, plus a spare transistor. For our GaN on SiC HEMT devices then the evaluation kit will either be for an IGNxxxx part which is a transistor that is partially matched within the transistor package to 50Ω or else it will be for an IGTxxxx device which is fully matched to 50Ω within the transistor package.

TRANSISTOR BIASING AND TURN-ON SEQUENCE

GaN HEMT devices are depletion mode transistors and so extreme care is needed to ensure that the correct biasing sequence is followed or else the transistor is likely to be destroyed. The transistor requires that a negative voltage be applied to the gate and that this must be applied before any positive voltage is applied to the drain. Thus two separate power supplies are required, one to supply a negative voltage to the gate and one to supply a positive voltage to the drain. Although both negative and positive voltage supplies are required for our evaluation kits, this is not necessarily a requirement in a customer's production amplifier as it is possible to use a Gate Pulsing and Sequencing (GPS) circuit to automatically apply the correct bias sequence to the device and set the required quiescent current in a fail-safe manner while at the same time only requiring a single positive voltage power supply. Full details of our GPS circuit can be found in Integra's Application Note 004.

The following sequence should be followed when testing the transistor:

1.. Ensure that the test bench presents good 50Ω source and load impedances to the evaluation kit with, ideally, around 30dB return loss. The output must have a load capable of handling ~3dB more power than both the rated peak output power and the average output power of the transistor.
2. Check the screw torque on the transistor clamp to ensure that the clamp has not loosened during shipment. The screws should be torqued sequentially to between 6-8 in/lbs.
3. The gate bias supply voltage should be adjustable over a range of at least -5V to -2V. The positive terminal of

the gate supply voltage must be connected to the test fixture ground, and the negative terminal connected to the blue bias lead as shown in Figure 1. **Applying a positive voltage to the gate will destroy the transistor!** Set the current limit on the gate supply to 100mA maximum. The gate supply must be able to source and sink current. At low RF power, the negative supply applied to the gate (BLUE terminal) will sink a current of a few mA due to the finite leakage current of the transistor. However, at high RF input power rectification of the RF input signal will occur due to the Schottky gate within the transistor. This causes the direction of the gate current to reverse and so now the gate supply must source current. Most bench power supplies cannot source and sink current. This problem can be solved by connecting a shunt resistor across the terminals of the gate power supply as shown in Figure 2. The value of R_{shunt} is determined by:

$$R_{shunt} < \frac{V_{GS,max}}{I_{GS,max}} \qquad (1)$$

For $V_{GS,max}$ = 4.5V and $I_{GS,max}$ = 10mA, then R_{shunt} < 450Ω. In Figure 2 a value of 67Ω was used. The resistor power rating should be > $V_{GS,max}$ x $I_{GS,max}$ i.e. >45mW in this example.

4. Set the gate supply voltage to -5V. Verify that the voltage on the transistor gate is -5V relative to the heat sink. Measure the resistance between the V_{DD} (RED) and ground (BLACK) terminals. You should measure around 10kΩ through the device drain if the gate supply voltage is properly applied since the channel is turned off.
5. Next connect the charge storage capacitor across the V_{DD} (RED) and GND (BLACK) terminals. This capacitor usually has a value of 4700μF. This capacitor is needed to minimize pulse droop when the RF signal is applied. After first ensuring that the drain power supply is switched off, connect the drain power supply to the test fixture with the positive output connected to the RED terminal and the GND connected to the BLACK terminal. Set the power supply current limit such that it, in conjunction with the charge storage capacitor, it can

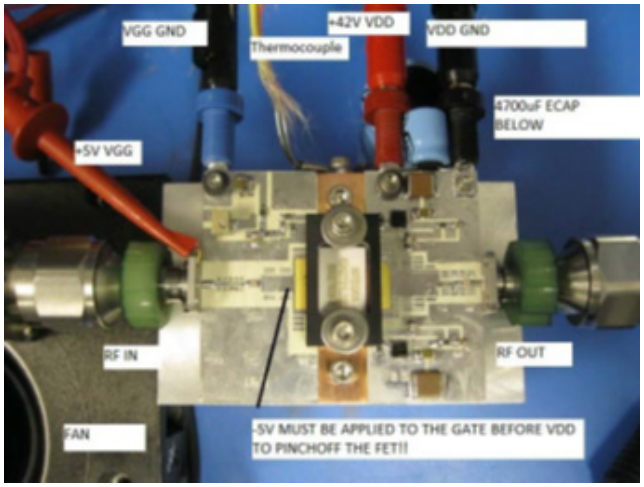

FIGURE 1: Detailed view of power supply connections to the test fixture.

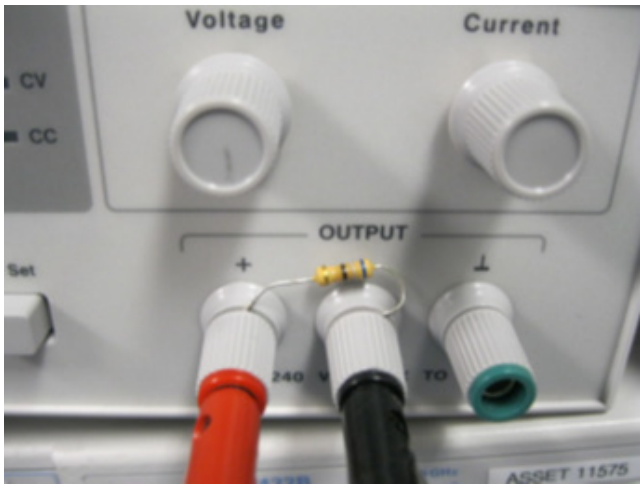

FIGURE 2: Configuring the gate power supply to both sink and source gate current.

handle the maximum peak current expected for the device. Next attach the power supply's voltage sense leads to the V_{DD} and V_{DD}, GND terminals if the power supply has this feature available. Ensure that the power supply is in its remote current sense mode. If the power supply does not have a voltage sense capability then connector a voltmeter across the RED and BLACK terminals on the test fixture and manually adjust the drain voltage during RF testing to compensate for any voltage drop.

6 Turn on the $+V_{DD}$ drain power supply and set V_{DD} to the value specified in the data sheet for the transistor. There should be less than 10mA of current drawn by the transistor from the drain power supply since the gate bias is at -5V to keep the device in pinch off.

7. SLOWLY increase the gate voltage (make less negative) from -5V until the quiescent current I_{DQ} specified in the transistor's data sheet is achieved. The gate voltage increment should not exceed 50mV to prevent overdriving the gate voltage, thereby inducing excessive drain current and potentially burning out the device. An Agilent E3610A power supply or equivalent is suitable. The gate voltage will typically be around V_{GS} = -2.7V to achieve the recommended I_{DQ} value. A spectrum analyzer should be connected at the output to ensure that no oscillations occur as the gate voltage is increased since oscillations can sometimes result in device destruction.

8. Turn on the RF input power starting at a low power (< 0.1W peak), and then increase until the desired output power is achieved. Correlation data is supplied with the clamped device. Please verify correlation with Integra's test results before changing the transistor. The detected RF output pulse should be monitored to ensure that no break up occurs as this may indicate the presence of an oscillation.

9 After the testing is complete turn off the $+V_{DD}$ drain supply voltage first but leave the RF applied for about 5 seconds to discharge the large drain charge storage capacitor. Next, turn off the RF power. Lastly, turn off the gate supply voltage.

DEVICE CORRELATION

The evaluation kit includes the test fixture, an electrolytic capacitor, two transistors, and our RF test data. One of the devices is already clamped into the test fixture. The device has been tested at Integra as installed, and should be used for correlation purposes. Please compare your measured data with Integra's RF data for the serial number installed in the test fixture and reconcile any discrepancies before removing or changing the transistor.

EFFICIENCY MEASUREMENT

Please note that the efficiency recorded in our test data is drain efficiency and not power-added efficiency. At L band there will be only a small difference – about two percentage points - between power added efficiency and drain efficiency since the transistors typically have about 18dB gain. However, at S and C band the difference is more significant since the gain is often around 13dB resulting in up to five percentage points difference. Please also be aware that the efficiency that is quoted is the efficiency during the pulse and not the efficiency over all time. Integra calculates efficiency from the product of the drain voltage and the average current drawn from the supply divided by the duty cycle. However, the transistor is drawing its quiescent current from the power supply when there is no RF signal applied and this effect is not

allowed for in our efficiency data. Consequently, our drain efficiency data underestimates the true efficiency. This effect can be significant, particularly for low duty cycle situations or if a high quiescent current is used (see Reference [1] for a practical example where it is shown that this effect results in the measured efficiency being six percentage points lower than the true value). Finally, it should also be noted that the drain current does not instantaneously drop to its quiescent value once the applied RF pulse is turned off. This is due to traps within the GaN epitaxial material; this effect is also referred to as a memory effect and will also contribute to the true efficiency during the pulse being higher than Integra's measured value.

TEMPERATURE COMPENSATION

The test fixture does not incorporate thermal compensation of the quiescent drain current. The gate bias voltage may need to be readjusted to maintain a constant I_{DQ} if testing with large variations in ambient temperature.

COOLING

The transistor will dissipate power and requires adequate cooling. As a minimum a biscuit-fan model BT2A1 or equivalent should be provided. This fan can provide 22CFM of airflow over the fins of the heat sink. A #4-40 UNC threaded screw hole is located on the copper carrier underneath the transistor to monitor the flange temperature. The typical flange temperature for RF testing is 30°C±5°C.

CHANGING THE TRANSISTOR

1. **The transistor is sensitive to ESD, and should be handled and tested in an ESD protected environment.**
2. Thermal grease was used for testing this part. Assuming that the heatsink of the test fixture has been cleaned, then only a small dot of grease 0.03-0.04" in diameter should be applied in the center of the slot. Do not use an excessive amount of grease. The grease pattern after transistor removal should not extend by more than 0.25". The correct amount of grease is required to obtain a thin coat that will not degrade electrical contact. Use Wakefield 120 [2] or equivalent thermal grease.
3. . Make sure that the clamp is properly seated on the top of the flange, and that the screws are torqued sequentially to between 6-8 in/lbs.

REFERENCE

1. Daniel Koyama, Apet Barsegyan, John Walker, "Implications of Using kW-level GaN Transistors in Radar and Avionic Systems", COMCAS Conference, Tel Aviv, Israel, 2-4 Nov, 2015.

2. www.wakefield-vette.com/resource-center/downloads/brochures/thermal-management-accessories-wakefield.pdf