150 V-Bias RF GaN for 1 kW UHF Radar Amplifiers

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***Abstract* — A 1 kilowatt pulsed RF amplifier operating at 150 V for radar applications in the UHF frequency band from 420 MHz to 450 MHz is presented. GaN HEMT devices with 600 V breakdown voltage are becoming ubiquitous in power conversion applications operating from kHz to a few MHz, but they have never been considered for RF applications in power amplifiers. This paper explores the advantages in high power RF amplifiers that employ a high voltage GaN technology operating above the industry standard of 50 V. The signal is a pulse of 100 µs width and 10% duty cycle. The power amplifier is based on a specifically designed RF GaN technology that can operate at 150 V bias. The RF GaN transistor has breakdown voltage in excess of 500 V and peak iron (Fe) doping in the buffer layer in excess of 10^{18} cm^{-3}. The single-ended 150 V RF GaN device utilizes three dice of 15 mm gate periphery assembled in a standard ceramic package. It achieves 1 kW output power across the band, with >70% drain efficiency without pulse gating during radar transmitter receive mode.**

Index Terms — amplifier, high efficiency, high power, high voltage 150V, GaN, UHF, radar.

I. Introduction

Notwithstanding the rapid progress in solid-state RF power technologies over the last decade or two since the advent of the wireless communication age, several high power applications in radars and in the industrial, scientific and medical (ISM) domain still rely on vacuum tube technology for the output stage of the transmitter. Unlike silicon RF power technology, Gallium Nitride (GaN) High Electron Mobility Transistors (HEMT) have unique and desirable attributes which are so well recognized and documented in the technical literature, allowing it to be long heralded as a replacement for vacuum tube devices. Such a technology could be used in high power RF amplifiers for applications in UHF weather radar, long-range tracking radar, particle accelerators, microwave sintering and other ISM applications, or as vacuum tubes replacement in general. However, commercially available GaN RF technology operates at power levels and operating voltages comparable to or slightly better than what is achievable with ubiquitous silicon RF power transistors. In order to produce a very high power RF transistor e.g. >1 kW with solid-state devices requires either a very high current or a very high voltage. A large current implies a large gate periphery, and hence chip size, which equates to high cost as well as a low value of load impedance which are both undesirable. High voltage, on the other hand, has no adverse impact on die size or cost other than device design difficulty. High voltage operation maintains high load impedance, but it also increases the dissipated heat. Heat can be a problem in CW operation, but less so in pulsed operation.

A 1st report of RF GaN devices operating at 75 V and 100 V at UHF frequencies with 250 W output power appeared in reference [1]. Breakdown voltage for these RF devices were 250 V and >500 V, respectively. Optimization of the 2nd and 3rd harmonics impedance match yielded efficiency of 80% and 75% respectively. A 2nd publication on RF GaN devices operating at 125 V in UHF band with very promising results appeared in reference [2]. Extensive RF burn-in tests at 125 V to address the reliability of this technology is reported in [3]. The target application for this earlier work was spaceborne Synthetic Aperture Radar subsurface imaging, and the devices were operated primarily at 75 V or 100 V. One device platform from ref. [2] was demonstrated to operate successfully at 150 V to achieve > 400 W output power from a 15 mm gate periphery at the spot frequency of 430 MHz.

For the present article 3x 15 mm GaN HEMT dice have been combined in a ceramic package to achieve 1 kW across the band from 420 MHz to 450 MHz; it achieves greater than 1 kW output power in pulse operation with 24 dB gain and > 70% drain efficiency corresponding to a power density of greater than 20 W/mm. The choice for the 420-450 MHz band is based on the fact that it is an ISM band used for many other applications; but it is high enough that 600 V silicon devices used primarily in power management cannot effectively operate. Although 1 kW output power is modest by today's standards what is impressive is that it is achieved with only 45 mm total gate periphery at 150 V bias. Moreover, this 1 kW has load impedance of > 10 Ω so there is plenty of scope to achieve 2 kW output power with a load impedance > 5 Ω and easy to match to 50 Ω. One way to realize such a 2 kW GaN transistor is to use 3x 150V RF GaN die of 30 mm in the same package as the 1 kW. Given the relatively high load impedance for this device, production yield in a manufacturing line is also expected to be good. Potentially, 4 kW output power could be achieved with load impedance of 2.5 Ω simply by combining 6x 30 mm chips in a larger, dual lead package. To support this statement in Fig. 1 we show a picture of the 3x chip 1 kW device studied in this work (top side of the picture, next to the coin of a US penny) with a dual lead package that can fit 6x similarly sized chips (bottom side of picture) which was designed for a different application and is shown for comparative purposes only (this particular device fits 7 chips as they are slightly smaller than the 150 V ones).

This 150 V RF GaN technology can replace vacuum tube devices as it can achieve the same output power, it has higher efficiency, better reliability typical of solid-state technology,

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no need for kV power supplies, and benign failure where one failed device does not shut down the entire system.

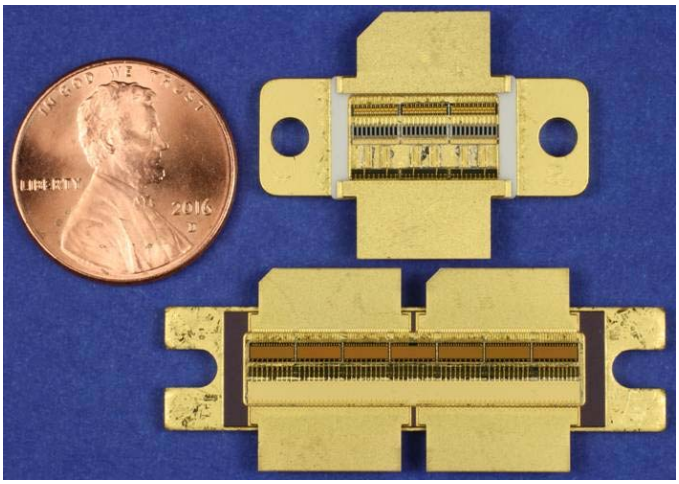

Fig.1. Comparison of the 1 kW 150 V device with 3 GaN chips (top side of picture) with a generic device housed in a dual lead package that can fit 6x similarly sized dice (bottom side of the picture).

II. RATIONALE FOR HIGH VOLTAGE RF GAN

Equation (1) gives the optimum load impedance of a class B amplifier given its operating voltage V_{DD} and the output power P_{RF} where V_K is the transistor knee voltage:

$$R_L = \frac{(V_{DD} - V_K)^2}{2\,P_{RF}} \qquad (1)$$

The output power of the transistor P_{RF} is proportional to the operating voltage V_{DD} and the transistor maximum current IDS_{MAX} as given by equation (2):

$$P_{RF} = \frac{1}{4}(V_{DD} - V_K)\, IDS_{MAX} \qquad (2)$$

Output power can be increased by increasing the maximum current and gate periphery of the transistor. The drawback is that the parasitic capacitances intrinsic to the transistor also increase making it harder to operate the device at higher frequencies; the parasitic capacitances also lead to low impedance which makes impedance matching harder to accomplish. Additionally, the drain-source capacitance C_{DS} is in parallel with R_L; therefore the equivalent impedance seen by the current generator is $R_L / (1 + j\,\omega\, R_L\, C_{DS})$. This shows how larger transistors yield lower load impedance.

Alternatively, output power can be increased by increasing the operating voltage V_{DD}. Thus, for a given output power, a smaller (gate periphery) transistor is needed which results in lower parasitic capacitances and higher impedance, both of which are very desirable. Neglecting the knee voltage of the transistor for simplicity, it can be calculated that with output power P_{RF} = 1 kW going from a supply voltage V_{DD} of 50 V to 150 V increases the load impedance R_L from 1.25 Ω to 11.25 Ω. The corresponding transformation ratio for a match to 50 Ω improves from 40x to only 4.4 x which is less lossy.

A device designed to operate at higher voltage requires a higher breakdown voltage, typically accomplished with a longer drift region and a modification of the epi structure for Gallium Nitride (GaN) devices and doping level in Silicon devices such as LDMOS. The modification for higher breakdown voltage results in a higher on-resistance (RDS_{ON}) of the device which is reflected in an increased knee voltage V_K. Tripling the operating voltage could lead to a 3x increase or more in the knee voltage V_K (see equations 4 and 7 in [4] for the 2x case). The maximum drain current is also slightly reduced, but not by a factor 3x. Therefore from equation (2) we derive that a 3x increase in operating voltage leads to higher output power, although a bit lower from the 3x ideal factor. The maximum efficiency of a class B amplifier with optimum load match conditions is then given by equation (3)

$$\eta_B = \frac{\pi}{4}\left(1 - \frac{V_K}{V_{DD}}\right) \qquad (3)$$

We can see that if increasing the operating voltage by 3x leads to a 3x increase in the on-resistance or knee voltage of the device, the maximum efficiency in a class B amplifier is unchanged. The key to achieving higher output power without sacrificing efficiency is to design the transistor for higher voltage operation while minimizing the impact on the on-resistance or knee voltage of the device. This objective is very hard to achieve with silicon technology, so that 100 V VDMOS or LDMOS can only competitively operate at sub 100 MHz frequencies. That's also the reason why 50 V LDMOS is only used up to L-band and for S-band 28 V LDMOS is used. With GaN operated at 150 V a new exploratory research path is being investigated and the results reported in the next section are very encouraging.

The AlGaN/GaN on SiC devices used in this research have been designed by varying the iron (Fe) content in the buffer layer of the epi-layer stack as reported in [2]. Another device engineering parameter to achieve 600 V breakdown voltage is the gate-drain extension, which is also varied from 4 µm to 9 µm. Extensions and height of the field plates are also important elements of the design. Measured data of the 3-terminal breakdown voltage are reported in Fig. 2. Gate-source junction is biased at -5 V.

Results show that BVDSS increases when increasing iron (Fe) concentration in the buffer layer, but clearly the gate-drain extension of the drift region is the key parameter of the design. Peak iron (Fe) concentration in the buffer and details of the field plates do affect the device's reliability and its RF performance.

The devices used in the present work correspond to the design yielding 600 V breakdown voltage in Fig. 2.

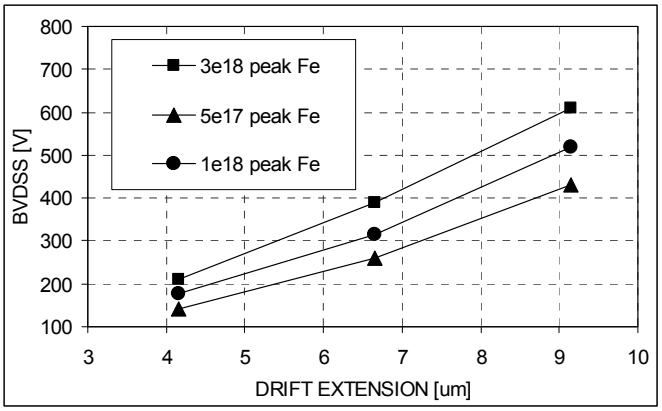

Fig.2. BVDSS vs. drift region length and peak Fe concentration in the buffer layer of a GaN HEMT.

III. 1-kW UHF Amplifier With 150 V GaN

The assembly configuration inside the package for the 150 V 1 kW device is shown in Fig. 3. The 1 µm gate-length transistor is housed in a CuW ceramic package with thermal conductivity of 180 W/m-°K and 60-mil thickness. The device uses an input LC resonance to increase the input impedance and the drain is bonded directly to the output transistor lead. This direct bonding allows for fundamental and harmonic tuning outside the transistor package. Thick-film series input resistors are used to enhance stability. Metalized substrates in the input section allow longer bond wires to achieve the required inductance. The 15mm transistor consists of 80 gates, each 190 µm long.

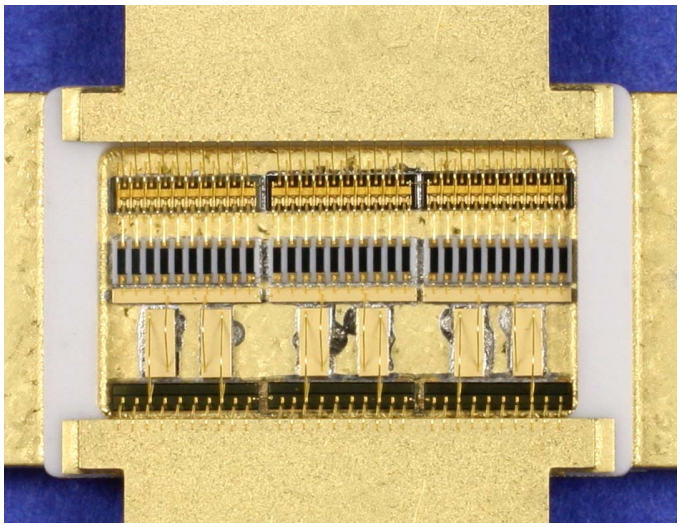
Fig.3. Close-up view of the 150 V 1 kW device with 3 GaN chips positioned next to the output package lead (top side in the figure).

The test environment uses a test fixture with fixed tuned input and output load impedances. For the output match, the test circuit uses a drain bias line section adjusted in length to affect the impedances at the harmonics. The fundamental frequency is matched with shunt capacitors placed along a 50 Ω line at appropriate distances from the device to optimize the fundamental frequency load. For the input section, the fundamental frequency is also matched with shunt capacitors placed along a 50 Ω line at appropriate distances from the device. Additionally, external slug tuners are used to optimize input return loss and output load match to 50 Ω across the band. Therefore the 1 kW circuit design is not complete yet and work to finalize the circuit is still in progress. In particular, further optimization of the harmonic terminations might result in yet better efficiency data [5]. A picture of the test fixture with the 1 kW device bolted down is reported in Fig. 4. Forced air cooling is applied during test through a fan positioned next to the extruded Aluminum heat sink located underneath the text fixture assembly. 90 mA quiescent current and 150 V bias was used during RF characterization. The RF input signal has 100 µs pulse width and 10% duty cycle.

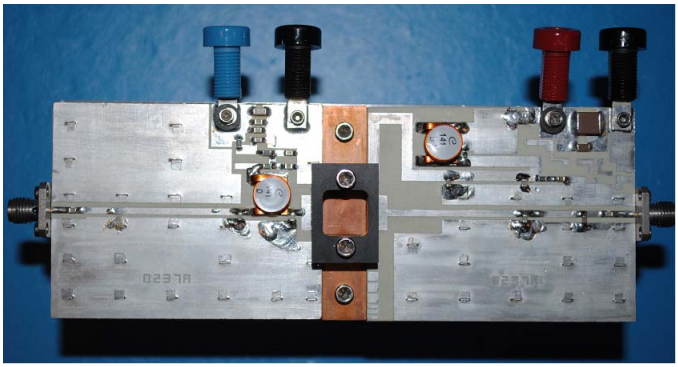
Fig.4. Picture of the test fixture for the 1 kW GaN device. Input and output matching consists mainly of 50 ohm transmission lines with shunt capacitors to tune first, second and third harmonics.

In pulse radar transmitter operation the quiescent current is removed during the off cycle of the pulse to reduce noise interference in the receiver which also improves amplifier efficiency; however, in our RF characterization setup it was kept constant at 90 mA. Frequency was varied from 420 MHz to 450 MHz. RF data for power gain and drain efficiency versus output power are shown in Fig. 5 across the four frequencies for the case where the duty cycle is 10%, which corresponds to a pulse period of 1ms. At 1 kW output power, power gain is 24.5 dB across the band and efficiency ranges from 73% to 78%. Saturated power is almost 1.1 kW across the band.

Subsequent measurements were taken with a duty cycle of 5% and 2% whereas the pulse width was kept at 100 µs. Data for power gain and drain efficiency versus output power when the duty cycle is 5%, corresponding to a pulse period of 2 ms, are shown in Fig. 6 across the four frequencies. Last, data shown in Fig. 7 are for the case where the duty cycle is 2%, which corresponds to a pulse period of 5 ms.

The overall trend is similar to the case with 10% duty cycle. The data shown in Figs. 5, 6 and 7 show almost the same efficiency, gain and output power versus pulse duty cycle, suggesting that the junction temperature of the device is not

affecting the RF performance even with the reported >20 W/mm power density.

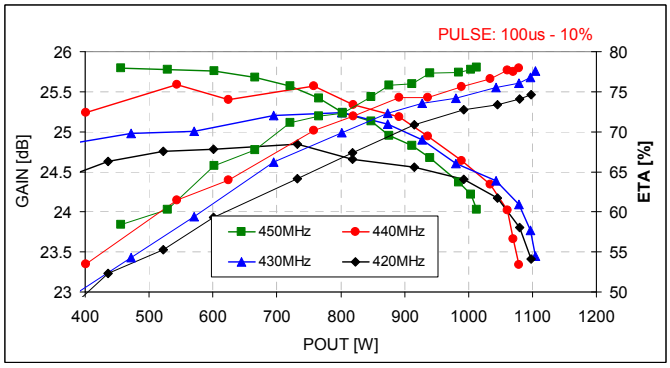

Fig.5. Power gain and drain efficiency vs. output power at 420 MHz, 430 MHz, 440 MHz and 450MHz at 150 V bias and 90 mA quiescent current. Pulse width is 100 µs; duty factor is 10%.

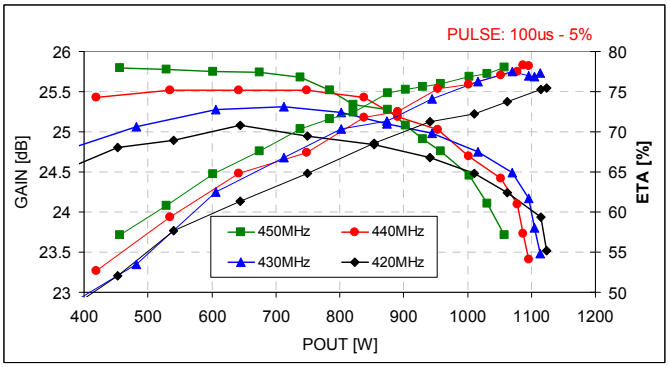

Fig.6. Power gain and drain efficiency vs. output power at 420 MHz, 430 MHz, 440 MHz and 450 MHz at 150 V bias and 90 mA quiescent current. Pulse width is 100 µs; duty factor is 5%.

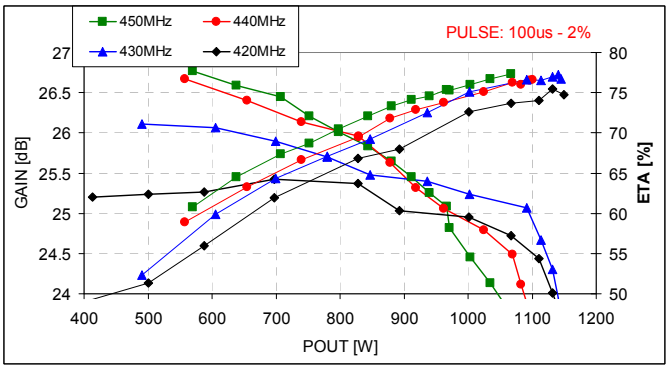

Fig.7. Power gain and drain efficiency vs. output power at 420 MHz, 430 MHz, 440 MHz and 450 MHz at 150 V bias and 90 mA quiescent current. Pulse width is 100 µs; duty factor is 2%.

With 1 kW output power and 75% drain efficiency the DC power is 1 kW / 0.75 = 1333 W and the dissipated power is 333 W or 111 W/die. Transient thermal modeling of the junction temperature based on the models described in ref. [6] and [7] has been done, as explained in more details in ref. [3].

For our 1 kW device the model predicts a peak junction temperature of 150 °C during the pulse on time when the case temperature is 80 °C, thus verifying operation in a safe regime. In our measurements the case temperature was set at 26 °C in which case the peak junction temperature reaches only 94 °C during the transient pulse.

IV. Conclusion

A 1 kW power amplifier operating at 150 V bias with >70% efficiency in UHF band has been reported. Load impedance is >10 Ω and it employs 3 GaN dice with only 45 mm total gate periphery. The data demonstrate the excellent capabilities of the 150 V RF GaN technology which is a serious contender for displacing vacuum tube devices in pulse radar applications. It is extrapolated that several kilowatt output power can be achieved by increasing the gate periphery to >100 mm. High voltage RF GaN technology also offers an interesting, yet still unexplored, proposition for high efficiency ultra-wideband power amplifiers. Furthermore, the larger voltage range may offer another degree of freedom in optimizing or improving the implementation of envelope-tracking (ET) in applications where high efficiency over a large dynamic range may be of interest.

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