Analysis of Bias Effects on VSWR Ruggedness in RF LDMOS for Avionics Applications

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Abstract — **A 210W RF LDMOS power transistor optimized for pulsed applications has been used to characterize VSWR ruggedness as a function of bias and gain compression. The ruggedness test used is the 10:1 VSWR load mismatch. The transistor, operated in class AB power amplifier, can deliver 210W of output power when biased at 32V (P3dB) or 36V (P1dB), having a minimum breakdown voltage of 85V. In both conditions the transistor passes 4:1 VSWR mismatch without degradation. We also found that when operated at 32V and 210W (3dB compression) the transistor passes 10:1 VSWR load mismatch without any degradation. On the contrary, when operated at 36V (1dB compression), the transistor either goes into catastrophic failure or it survives the mismatch test with a severe power rating degradation in excess of 5%. Measured electrical data and simulated junction temperature data help explaining the different results on the VSWR ruggedness.**

I. INTRODUCTION

In the present paper we characterize the effects of gate and drain bias on the transistor ruggedness as measured by the VSWR load mismatch test in high power RF LDMOS. VSWR is the ratio of the optimum load impedance for maximum power and the actual load impedance in a mismatch condition for a given frequency. In 10:1 VSWR output mismatch 67% of the output power is reflected from the load back to the transistor and only 33% is transmitted to the load [1]. A rugged transistor must be able to absorb and dissipate into heat this reflected power without suffering any damage or degradation. This is usually accomplished during the design stage of the transistor making sure that there is enough drain resistance to absorb the reflected power. In the case of RF LDMOS, this desirable feature is part of the optimization process in the drain engineering design. Usually, the drain engineering design aims at minimizing the on-resistance for a given breakdown voltage, for CW operation. If ruggedness is indeed another major constrain, as in the case of avionics or radar pulsed applications, more trade-off conditions must be taken into consideration.

Integra Technologies, Inc has designed its proprietary RF LDMOS transistor with a grounded Faraday shield to isolate the gate from the drain and therefore reduce the feedback capacitance Cdg, as shown in the drawing of Fig. 1. Integra's LDMOS technology also adopts an all gold metallization stack for maximum ruggedness and reliability.
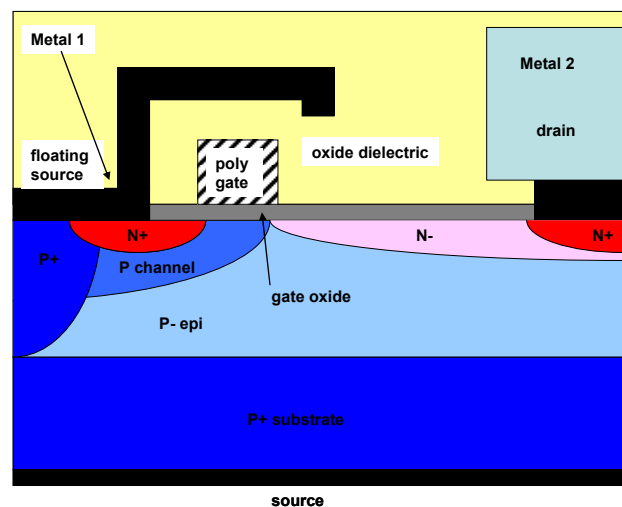

Fig. 1 Cross-section of an LDMOS design with Faraday Shield.

II. RESULTS AND DISCUSSIONS

A 210W single ended RF LDMOS transistor, designed and optimized for pulse signal operation, has been used to study the effects of gate and drain bias on RF ruggedness as measured by the die ability to pass a 10:1 VSWR load mismatch test. The transistor, suitable for avionics applications in the 1.0-1.1GHz band, has a minimum breakdown voltage of 85V, and is typically biased at 10mA or 50mA of quiescent current. The threshold voltage is about 3.5V. The on-resistance was measured on this large die at Vds=0.1V and Vgs=10V, yielding 0.25 ohms. The input and output capacitances were measured on this large periphery LDMOS chip using a capacitance meter by grounding the source (substrate of the die) and applying a 1MHz probe signal at the gate (with floating drain) and at the drain (with floating gate) respectively. Fig. 2 shows the input capacitance versus gate-to-source voltage, including the 200pF input match capacitor, and Fig. 3 shows output capacitance versus drain-to-source voltage.
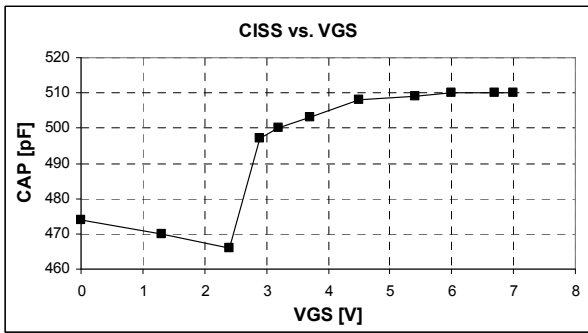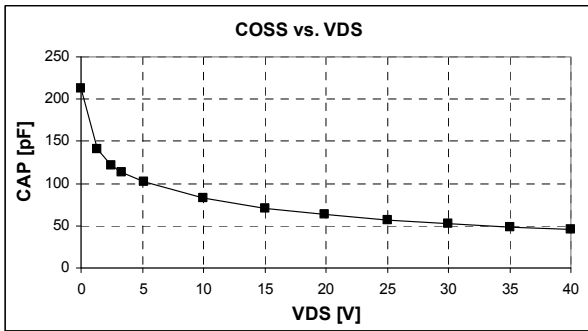
Fig. 2 Input capacitance profile.

Fig. 3 Output capacitance profile.

Fig. 4 Picture of one LDMOS die packaged with input match.

Fig. 5 Picture of two LDMOS dice in a single package with input match.

A single die in a standard LDMOS package with input match, delivers in excess of 200W output power when biased at either 32V or 36V. Notice that in this voltage range the output capacitance is almost constant at 50pF. Biased at a drain voltage of 32V, the output power of 210W is achieved with 3dB gain compression; with the drain bias at 36V, the same power level is now achieved at 1dB gain compression. Fig. 4 shows a picture of the transistor single die packaged with input match.
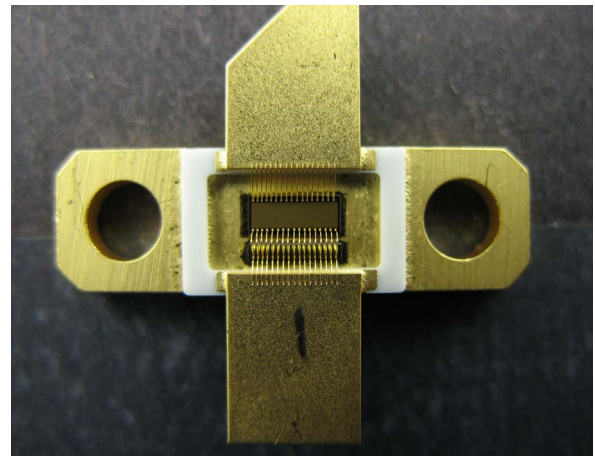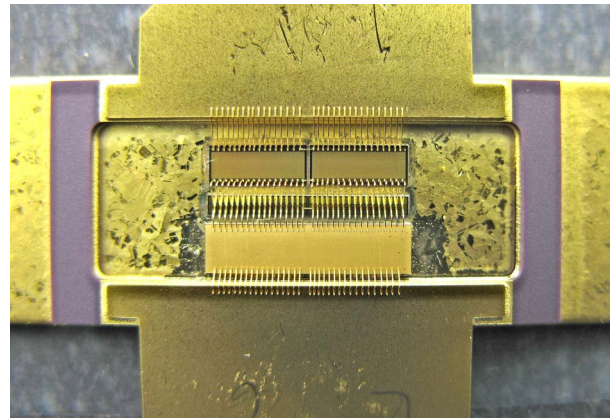
Fig. 5 shows a picture of a larger package with two LDMOS dice. In both cases the transistor passes a 4:1 VSWR load mismatch test, where 36% of the output power is reflected from the load back to the transistor [1]. This result confirms that the die has been designed to sustain a minimum amount of load mismatch in excess of 3:1 VSWR load mismatch.

Next the transistor ruggedness has been characterized for a higher level of load mismatch, such as 10:1 VSWR. This is considered a good measure of ruggedness test for most practical applications encountered in avionics and radar power amplifiers. Operated in class AB with a supply voltage of 32V and 10mA quiescent drain current, the RF LDMOS transistor has a 3dB output power of 210W, 60% drain efficiency, 13dB gain and it passes 10:1 VSWR load mismatch at all phase angles without any power degradation. Fig. 6 shows the gain and drain efficiency versus output power for this bias condition.
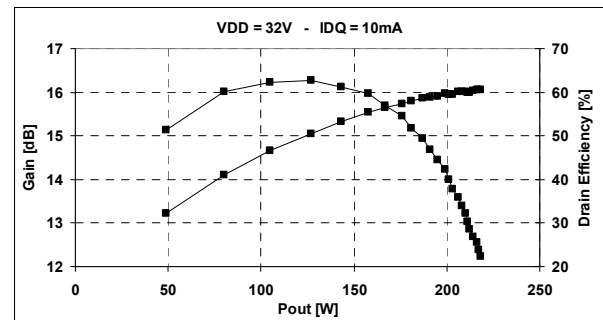

Fig. 6 Pulsed CW data at 1030MHz for gain and drain efficiency vs. output power for one LDMOS transistor biased at 10mA and 32V.

Similarly, two chips in a larger package biased at 32V and 20mA yield over 350W of output power 3dB into compression with 50% drain efficiency and 12dB gain. The RF data are shown in Fig. 7. The device still passes 10:1 VSWR load mismatch at all phase angles without degradation. The signal pulse has a duty cycle of 2% and is 50us long.
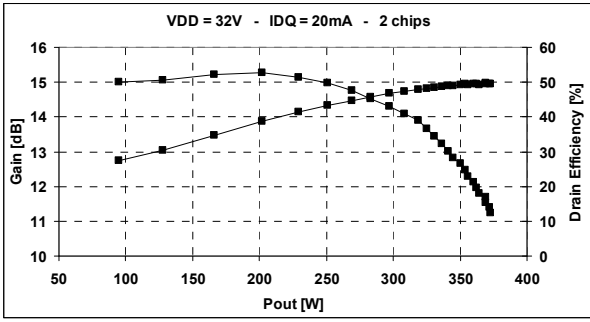
Fig. 7 Pulsed CW data at 1030MHz for gain and drain efficiency vs. output power for two LDMOS transistors in the same package biased at 20mA and 32V.

In Fig. 8 we report the effect of gate bias by increasing the quiescent current from 10mA to 50mA on the RF data, since both options are used in actual avionics applications. The supply voltage is still 32V. Notice that the output power compression feature is the same, but higher quiescent current yields a higher gain and lower efficiency, as expected.
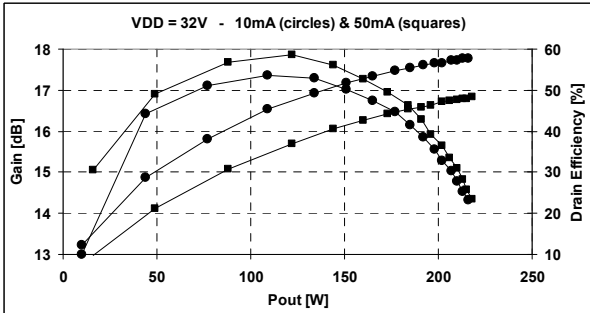

Fig. 8 Pulsed CW data at 1030MHz for gain and drain efficiency vs. output power for one LDMOS transistor biased at 32V for 10mA and 50mA quiescent current.

Next, the single chip in the smaller package has been tested at 36V with 50mA quiescent current and a 2% 50us pulse signal. Here 210W is the output power at 1dB compression and although the transistor can absorb a medium level of mismatch (it passes 4:1 VSWR at all phase angles without any appreciable degradation) it fails to pass a 10:1 VSWR load mismatch. Some transistor units pass the test at 36V, but with 5% to 10% degradation in the RF output power. In Fig. 9 it is shown the RF data at 32V and 36V for a direct comparison between the two cases. Although the power level of the transistor used in the 10:1 VSWR test is the same in the two conditions, the ruggedness results are very different and must be attributed to the different bias conditions, either the supply voltage or the quiescent current.

Since we use very short pulse signals, the thermal effects have been minimized [2]. In fact, the thermal time constant τ is found to be about 25us, based on the following information [3]: $\tau=(2h/\pi)^2/\alpha$, where h=75um (~3mils) after silicon wafer thinning, and α=0.92 cm^2/s is the silicon thermal diffusivity. Considering that the duty cycle of the pulse signal used in our measurements is 2%, the time between each pulses is 2.5ms with 50us pulse width. With such short pulse width and long inter-pulse intervals, the junction temperature has the time to relax to ambient temperature before a new pulse starts [4, p.243, case 2].
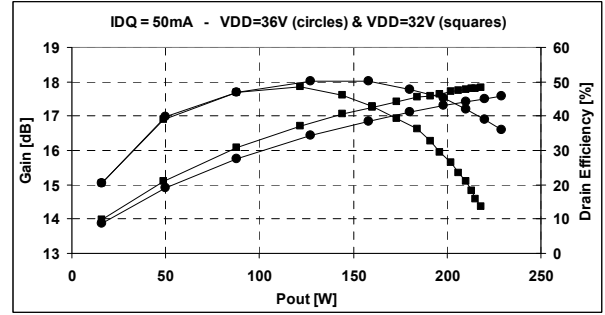

Fig. 9 Pulsed CW data at 1030MHz for gain and drain efficiency vs. output power for one LDMOS transistor biased at 50mA quiescent current at 32V and 36V.

With the pulse width (50us) longer than the thermal time constant (25us), when the pulse signal is on, the junction temperature increases to its peak value, estimated to be about 82 °C if the transistor is biased at 10mA 32V, whereas it is about 126 °C when biased at 50mA 36V. See Table I for the measured electrical data and the extracted dissipated power and junction temperature increase in a matched load condition. We have used a die thermal resistance R_{TH} of 0.126 °C/W [calculated based on ref. 4, p. 234 and die layout data] and a package thermal resistance of 0.25 °C/W. Therefore from the dissipated power the junction temperature increase is $\Delta T = P_{diss} R_{TH}$.

TABLE I
MEASURED ELECTRICAL DATA WITH MATCHED LOAD AND ESTIMATED
JUNCTION TEMPERATURE INCREASE.

IDQ [mA]	Pout [W]	Vdd [V]	Pin [W]	Id [A]	Pdiss [W]
10	210	32	10	11	152
50	210	36	4	13.2	269.2

IDQ [mA]	Rjc [C/W]	ΔT [C]	Rpkg [C/W]	Tc [C]	Tj [C]
10	0.126	19.2	0.25	63	82.2
50	0.126	33.9	0.25	92.3	126.2

From the measured electrical data is it worth noticing that the higher quiescent current leads to a larger drain current drawn from the supply voltage source and to about 120W difference in dissipated power between the two cases. The junction temperature difference in the two cases is about 45 °C. Although the estimated peak junction temperature seems pretty high in both cases, the junctions operates at these temperatures for a very short time period, since the device is operated in pulse conditions with 2% duty cycle. Because of the pulsed conditions, the average junction temperature is only a few degrees above the room temperature of 25 °C [4] and it cannot have a significant contribute to the different ruggedness behaviour reported in our measurements.

Based on our data and test conditions we attribute the different ruggedness reported in the different operation of the transistor to the different voltage swing and its relationship with the onset of avalanche breakdown at high VDS. Our measurements show that, although higher voltage operation leads to higher saturated power, the transistor's ruggedness at high levels of load mismatch is compromised faster than the

improvement in output power. A lower supply voltage yields the same power level achieved with a higher voltage (although at different gain compression levels), but with a better ruggedness measure. The compromise is that the same power rating is achieved at a higher level of gain compression and therefore of nonlinearity. It is well established that RF power transistors operated at higher supply voltage lead to higher output power [2]. However, unless the transistor is redesigned for a higher voltage operation, i.e. with a higher breakdown voltage, over-biasing leads to die failure or accelerated performance degradation.

We want to emphasize that for Integra's LDMOS, the optimization of the die design process, through drain and channel engineering, and layout techniques, is driven by achieving highest pulse peak power operation with safest ruggedness margins, and not best linearity in CW operation as is done by other manufactures whose expertise remains focused on base stations applications.

Although the paper highlights a measurable ruggedness difference in high VSWR load mismatch for Integra's LDMOS when operated at 32V versus 36V, we want to remind the reader that medium levels of VSWR load mismatch (4:1) are indeed absorbed without any measurable degradation in both supply voltage operations and at power levels well above the 100W mark. For comparison, it is also noteworthy that the BJT (Bipolar Junction Transistor) technology, traditionally used for avionics and radar applications, is typically tested to pass a 5:1 VSWR load mismatch at power levels below 100W [5], with 3:1 VSWR being more typical at higher power levels [6]. RF LDMOS, on the other hand, has shown much higher ruggedness measures at higher power levels, and it can also be easily designed or optimized to meet more stringent ruggedness conditions.

III. CONCLUSIONS

The ruggedness of high power (>200W) RF LDMOS transistors to VSWR load mismatch has been characterized. We used a 210W RF LDMOS die manufactured by Integra Technologies, Inc. It is an all gold LDMOS technology specifically designed to address requirements for avionics and radar pulsed applications. The high power transistor (>200W) can be biased at either 32V or 36V, and in both cases it is able to survive a medium amount of load mismatch, such as 4:1 VSWR. However, we found that at higher levels of load mismatch, such as 10:1 VSWR, the transistor passes the test when operated at 32V but at 36V it either fails catastrophically or it survives with severe degradation, most likely due to excessive drift of the on-resistance. Finally, when biased at 36V and used at a power level corresponding to peak gain, typically around 150W, the transistor does pass the 10:1 VSWR load mismatch at all phase angles without any degradation.

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