Solid-State RF Power Amplifiers for ISM CW Applications Based on 100 V GaN Technology

Gabriele Formicone[1], Jeff Burger[1], James Custer[1], Gianni Bosi[2], Antonio Raffo[2] and Giorgio Vannini[2]

[1]Integra Technologies Inc., 321 Coral Circle, El Segundo, CA, 90245, USA
[2]University of Ferrara, Department of Engineering, 44122 Ferrara, Italy

***Abstract*— A novel solid-state power amplifier technology for RF power sources used in various industrial, scientific and medical (ISM) applications is presented. The prototype devices reported for this paper achieve 200 W CW saturated output power with 80% drain efficiency at 430 MHz and 110 W at 915 MHz. Unlike ubiquitous 50 V solid-state transistor technology, the data we present explore 75 V and 100 V bias operation in UHF band with GaN devices which have the potential of achieving >70% efficiency at kilowatt power level by properly designing and sizing the active devices. Microwave sintering, particle accelerators and magnetic resonance imaging equipment at UHF or L-band are the most likely beneficiary of the technology introduced in this paper.**

Keywords*— accelerator, amplifier, high efficiency, GaN transistor, microwave, sintering.

I. INTRODUCTION

Several industrial applications exist at ISM frequencies spanning from VHF to UHF to L-band and S-band (13.56 MHz, 325 MHz, 430 MHz, 650 MHz, 915 MHz, 975 MHz, 1300 MHz, 2450 MHz, 2856 MHz etc...) where high power solid-state RF amplifiers could replace traveling wave tubes such as klystrons or magnetrons if high CW power or high average power in pulse mode is achievable [1]. RF amplifiers with high CW or average pulse power ranging from a few kilowatts to tens of kilowatts are required for RF heating microwave sintering or curing as used in bulk powder drying or in the ceramic and metallurgical industry. Even the petroleum industry can make use of electromagnetic energy to reduce viscosity and facilitate percolation for gravity-assisted drainage. Studies have shown that targeted heating by electromagnetic energy is a more effective process compared to alternative thermal heating [2]. These studies suggest that higher frequencies and continuous wave operation is more effective than lower frequencies and pulse operation. Another area where high efficiency RF sources are desired is particle accelerators for emerging applications in energy and environment [3]. Incumbent non-solid-state technology has the benefit of very high power capability but the kilovolt range power supply required is extremely bulky, costly and the amplifier efficiency is limited to 65% at best; solid-state RF sources capable of operating at higher efficiency are desirable to reduce operating costs and make the technology viable from a business perspective. Even the US Department of Energy is actively interested with innovative solutions in high power RF sources for particle accelerators with high efficiency [4]. Absence of dangerous kilovolt bias level, longer lifetime and stable gain with aging, easier and quicker maintenance, possibility of reduced power operation in case of failure and the possibility of fitting different power levels with the same building block or amplifier module are among the advantages that solid-state RF sources provide compared to vacuum tube technology [5]. In terms of operating costs, the price of vacuum tubes increases over time as fewer and fewer manufacturers remain in the business (which also threatens their long-term availability) whereas due to the continuous push from the wireless communications market the availability of solid-state devices continues to grow and their $/W ration continues to decrease. Solid-state RF high power sources for particle accelerators operating at 352 MHz have already been successfully demonstrated at SOLEIL [6] a decade ago and since then in other research facilities around the world. Nowadays solid-state solutions based on LDMOS technology can provide from 350 W to 500 W CW power in a dual lead package transistor but efficiency is limited to ~50% or ~60% at best in CW mode at 915 MHz [7, 8]. Some VDMOS devices are available with breakdown voltage up to 300 V but their frequency of operation is limited to only the VHF region. In this paper we explore a high voltage gallium nitride (GaN) based solution operated in CW mode at 75 V and 100 V bias which has the potential of achieving very high power levels with efficiency in the 80% range. Our demonstration devices have been characterized at 430 MHz and 915 MHz.

II. RATIONALE FOR HIGH VOLTAGE RF GAN

Fundamental power amplifier analysis proves the rationale for the suggested approach. Equation (1) gives the optimum load impedance of a class B amplifier given its operating voltage V_{DD} and the output power P_{RF} where V_{knee} is the transistor knee voltage (typically 10% to 20% of V_{DD} in GaN RF devices and 20% to 30% of V_{DD} in LDMOS):

$$R_L = \frac{(V_{DD} - V_{knee})^2}{2\,P_{RF}} \qquad (1)$$

Neglecting the knee voltage of the transistor for simplicity, it can easily be calculated that with output power P_{RF} = 1 kW going from a supply voltage V_{DD} of 50 V to 100 V increases the load impedance R_L from 1.25 Ω to 5 Ω. The corresponding transformation ratio for a match to 50 Ω improves from 40x to only 10x which is significantly less lossy. The output power of the transistor P_{RF} is proportional to the operating voltage V_{DD} and the transistor maximum current IDS_{MAX} as given by equation (2) after accounting for the knee voltage V_{Knee}:

$$P_{RF} = \frac{1}{4}(V_{DD} - V_{Knee})\ IDS_{MAX} \qquad (2)$$

Output power can be increased by increasing the maximum current or gate periphery of the transistor. However, the drawback is that the parasitic capacitances intrinsic to the transistor also increase making it harder to operate the device at higher frequencies due to bigger RF losses; the parasitic capacitances also lead to a low impedance regime which makes impedance matching hard to accomplish. For instance, the output drain-source capacitance C_{DS} is in parallel with R_L given by equation (1) above so that the equivalent impedance seen by the current generator is $R_L / (1 + j\ \omega\ R_L\ C_{DS})$ proving that the larger the size of the transistor the lower the load impedance. Alternatively, output power can be increased by increasing the operating voltage V_{DD}. Thus for a given output power a smaller (gate periphery) transistor is needed which results in lower parasitic capacitances and higher impedance, both of which are very desirable. A device designed to operate at higher voltage however requires a higher breakdown voltage, typically accomplished with a longer drift region and a modification of the epi structure for Gallium Nitride (GaN) devices or doping level in Silicon devices such as LDMOS. The modification for higher breakdown voltage results in a higher on-resistance (RDS_{ON}) of the device which is reflected in an increased knee voltage V_{Knee}. Doubling the operating voltage could lead to a 2x increase or more in the knee voltage V_{knee} (see equations 4 and 7 in [9]). The maximum drain current is also slightly reduced, but not by a factor 2x. Therefore from equation (2) we derive that a 2x increase in operating voltage leads to higher output power, although a bit lower from the 2x ideal factor. The maximum efficiency of a class B amplifier operating under optimum load match conditions is then given by equation (3)

$$\eta_B = \frac{\pi}{4}\left(1 - \frac{V_{Knee}}{V_{DD}}\right) \qquad (3)$$

We can see that if increasing the operating voltage by 2x leads to a 2x increase in the on-resistance or knee voltage of the device, the maximum efficiency in a class B amplifier is unchanged. The key to achieving higher output power without sacrificing efficiency is to design the transistor for higher voltage operation while minimizing the impact on the on-resistance or knee voltage of the device. This objective is hard to achieve with silicon technology, so that 100 V VDMOS or LDMOS are only competitive at sub 100 MHz frequencies as briefly mentioned in reference [5]. That's also the reason why 50 V LDMOS is only used up to L-band and for S-band 28 V LDMOS is used. For instance, in reference [10] a 1 kW transistor for pulse S-band airport radars operating at 50 V is described for the 2.7 - 2.9 GHz band with 56% power added efficiency and 11 dB gain. In this exploratory research work we have taken 15 mm and 18 mm GaN transistors which can operate at 75V and 100 V bias and characterized them in CW operation at 430 MHz and 915 MHz. We first report data on a prototype 110 W CW linear output power device using GaN transistors that operate at 75 V in class AB with efficiency of >70% at 915 MHz and later a 200 W CW device at 430 MHz. We have used 915 MHz to compare our results in narrow band against results available with state-of-the-art 50 V LDMOS technology. Also, 915 MHz rules out the older VDMOS technology that can operate at higher bias voltage. The results are significant because switch-mode amplifier techniques such as class E and F can increase efficiency towards a much desired 80% level and larger chips can definitely deliver higher output power than the 100 W devices we have evaluated. In reference [11] it is already demonstrated a power amplifier with greater than 80% efficiency using readily available VDMOS and LDMOS devices in the 325 MHz and 650 MHz frequency bands for particle accelerators. A similar approach would be applicable to the technology introduced in this article.

III. CW RF TEST RESULTS

We have assembled a GaN transistor without pre-match at the output. The input side is pre-matched with the resonance frequency at 890 MHz, so we were able to tune the devices at 915 MHz. A typical LDMOS or VDMOS device designed to operate at 50 V typically has a breakdown voltage of ~120 V, but GaN devices from several manufacturers tend to have a breakdown voltage from 150 V to over 200 V, opening up the possibility of biasing them at higher V_{DD} for higher output power and higher optimum load impedance R_L. Of course this is possible if the device is able to withstand operation at increased bias with good reliability. In order to keep the electrical and thermal stress of the device contained, we have used devices of smaller rather than larger gate periphery or power level. A prototype test fixture was built to test the devices at a single frequency of 915 MHz in class AB operation with 30 mA quiescent current; external tuners were used to match to 50 Ω at the fundamental frequency under different test conditions. No tuning of the harmonic frequencies has been done at this time. In all cases the device was bolted to a copper carrier within the test fixture for best heat dissipation during CW operation. The test fixture is then bolted to a copper chassis machined to allow water circulation for liquid cooling which ensured the copper base plate temperature next to the package flange was always in the 22 °C to 27 °C range.

In Fig. 1 on the next page power gain and drain efficiency versus CW output power are shown for device #1, which has BV_{DSS} approaching 200 V. Therefore the device was tested at 50 V and 75 V at a frequency of 915 MHz. By increasing the power supply voltage V_{DD} from 50 V to 75 V results in increased output power from 80 W to 110 W. Gain also increases by ~1 dB, but in both cases the peak efficiency is the same at 75%. This device has 18 mm gate periphery. In Fig. 2 power gain and drain efficiency versus RF CW output power are shown for device #2, which has BV_{DSS} in excess of 500 V. Therefore the device was tested at nominal 50 V and compared with operation at 75 V and 100 V at 915 MHz. This other device has 15 mm gate periphery. By increasing the power supply voltage V_{DD} from 50 V to 75 V and 100 V results in increased output power from 55 W to 90 W and to 110 W. Peak efficiency is ~65% for all three cases and it is lower than in device #1 because of differences in the drift region which is manifested in the different breakdown voltage. Following these considerations, it may be necessary to optimize the die design with a shorter drift region; re-adjust the location of the field plates, and increase the gate-gate spacing for a lower thermal

resistance. The package used has 60-mil thick CuW flange which results in a thermal resistance of 3 °C/W.

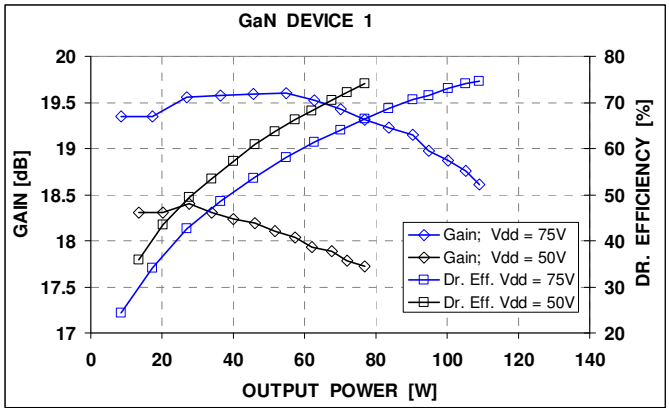

Fig. 1. Comparison of an 18 mm device at 50 V and 75 V operation; 110 W output power is reached with 75% drain efficiency and 18.5 dB gain at 75 V bias; frequency is 915 MHz. Die has 1 µm gate length.

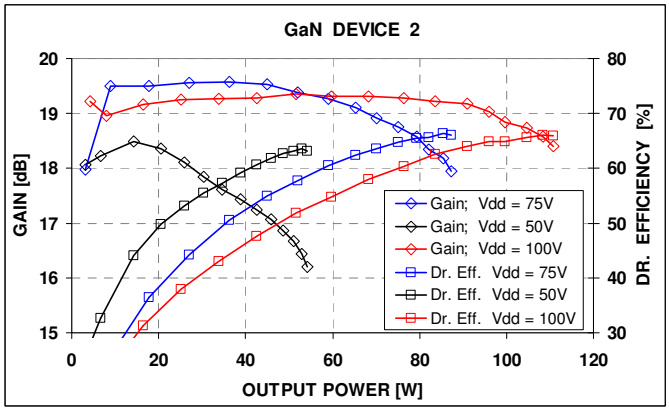

Fig. 2. Comparison of a 15 mm device at 50 V, 75 V, and 100 V operation; 110 W output power is reached with 65% drain efficiency and 18.5 dB gain at 100 V bias; frequency is 915 MHz. Die has 1 µm gate length.

Next the 15 mm die was assembled for narrowband RF tests carried out at 430 MHz which yield 80% efficiency and 200 W CW output power when operated at 100 V bias. The input side is pre-matched with the resonance frequency at 400 MHz and the output side is unmatched. A different test fixture was used in this case. Figs. 3 and 4 show measured RF data for such transistor (i.e., device #3). The data were taken at 75 V, 100 V and 125 V bias using only a cooling fan for heat dissipation. Data taken at 75 V demonstrate 80% efficiency and saturated output power is ~150 W CW, corresponding to a power density of 10 W/mm. Efficiency seems to degrade at 125 V, but the measurement might be effected by the increasing case temperature of the test fixture as no liquid cooling was used to ensure it remained at room temperature, and the test fixture was harmonically tuned (up to the 3rd harmonic) at 100 V so it might not have been optimized for 125 V. The normalized impedance ratios for the test fixture are measured at 100 V and de-embedded per the technique used in [9]. They are compared to the optimum load impedances for class E and F^{-1} switch mode amplifiers in Table 1.

TABLE 1: Comparison - Normalized Load Impedances
Inverse Class F and Class E versus Test Devices

	Class F^{-1}	Class E	100V TF
F1	1	1+j0.725	1+j0.19
F2	Open	-j1.785	0.06-j0.51
F3	Short	-j1.19	0.03-j0.19

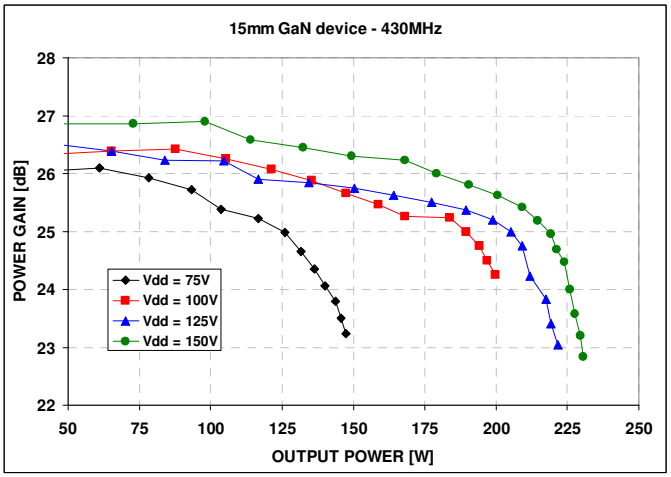

Fig. 3. Comparison of device #3 at 75 V, 100 V, 125 V, and 150 V operation. Saturated output power increases from 150 W to 200 W for supply voltage at 75 V and 100 V, and it saturates at 220 W and 230 W for the supply voltage of 125 V and 150 V; frequency is 430 MHz. Gate length is 1 µm.

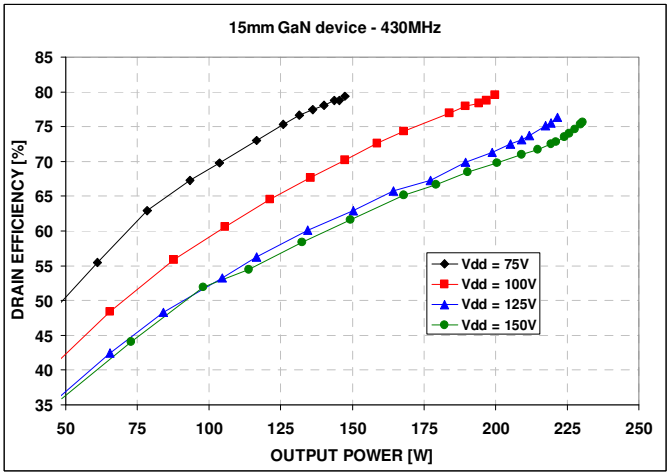

Fig. 4. Comparison of device #3 at 75 V, 100 V, 125V and 150 V operation. Peak drain efficiency is 80% for supply voltage going at 75 V and 100 V, and then it decreases to 76% with the supply voltage of 125 V and 150 V; frequency is 430 MHz and gate length is 1 µm.

Operation at 100 V bias appears to be a best compromise of saturated power of 200 W CW (13 W/mm CW power density) and efficiency still at 80%, but more work could show yet higher efficiency. In ref. [12] it is explained that 90% is achievable by tuning harmonics from 2nd to 5th (Table II, page 1467) order. The package used for device 3 has 40-mil thick CPC flange resulting in a thermal resistance of 2 °C/W; this is

better than in the samples used at 915 MHz. The analysis shows that the package can have a significant effect on R_{TH} and the overall RF performance. With increased bias it is important to prove that the GaN transistor is capable of sustaining the larger electrical stress and the best way to accomplish that is by analyzing the load lines when the device is operating as intended. That is discussed in the next section.

IV. Loadline Analysis

A unit cell of the device #1 with breakdown of 200 V was used to analyze its performance in a time domain measurement setup. Load line analysis with bias at 25 V, 50 V and 75 V was conducted to determine if raising the bias voltage would translate into deteriorated knee voltage and increased on-resistance. In GaN devices this effect can be pronounced and it is referred to as knee voltage walkout or DC-RF dispersion.

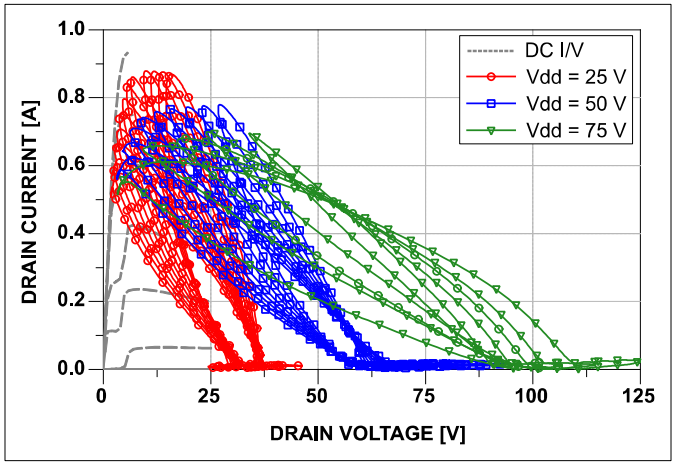

Fig. 5. Load line analysis of device #1 unit cell at 25 V, 50 V and 75 V with operation in class AB.

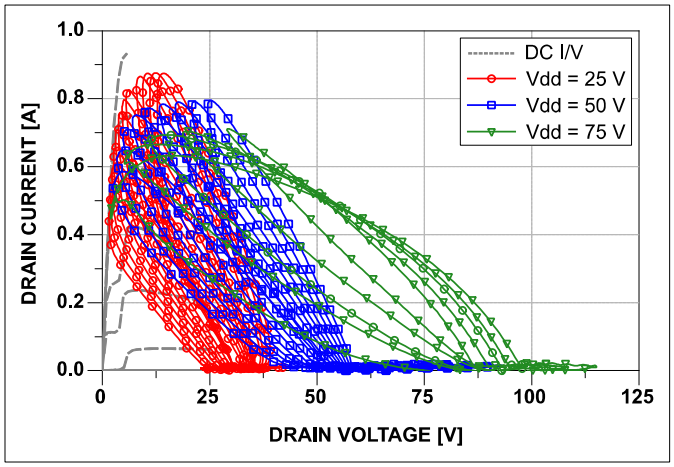

Fig. 6. Load line analysis of device #1 unit cell at 25 V, 50 V and 75 V with operation in class C.

For the load line analysis, we biased the device in class AB and class C so that we could ascertain whether or not operation at increased drain bias would be sensitive to the amplifier conduction angle. Data for class AB and C operation are shown in Figs. 5 and 6 respectively. Measured data show a reduction in saturated current as drain bias is increased from 25 V to 50 V to 75 V, but this effect is mostly attributed to the increased output power at increased voltage which translates into higher junction temperature of the device. Only air cooling was used in the load line measurements and it was found that the case temperature increased from 25°C to 45°C to 60°C when the bias voltage was increased. No significant difference is observed on knee voltage or on-resistance. The results are identical whether class AB or class C gate biasing was used.

V. Conclusions

The paper explores the possibility of utilizing solid-state GaN RF devices operated at 75 V and 100 V in CW operation for ISM applications at 430 MHz and 915 MHz such as magnetic resonance imaging, microwave sintering and particle accelerators. The results suggest that higher bias operation is a viable approach to achieve higher output CW power with efficiency greater than 70%. The prototypes utilized for this work achieve 110 W at 915 MHz and 200 W at 430 MHz, but the approach is scalable to larger or multiple transistors for higher power levels. Load line analysis on the device unit cell at increased bias demonstrated no increased DC-RF dispersion.

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