# A 130W LDMOS for 2.7-3.5 GHz Broadband Radar Applications

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***Abstract* — A 32V LDMOS technology with all gold metallization optimized for pulsed applications has been used to design a 130W discrete power transistor matched over the 2.7 - 3.5 GHz instantaneous frequency band, covering both commercial and military radar markets. The high power device, operated in class AB bias, with a 300us and 10% duty cycle pulse signal supplies a minimum of 130W of peak power with over 8dB gain and a minimum of 36% drain efficiency. The internally matched device is housed in a push-pull style package, but is used in a single-ended broadband text fixture matched to 50 Ω with hybrid combining. To the authors knowledge this is the first time that an LDMOS technology has successfully demonstrated acceptable performance over an 800 MHz bandwidth in the S-band radar application space.**

## I. Introduction

High power RF transistors are a key component in radar systems and advances in transistor technology can both significantly improve system performance and reshape the market landscape. Most radar transmitters operate over relatively broad frequency bands, segmented depending on the scope of the application. Most common frequency bands for S-band radars are the 2.7 – 2.9 GHz, 2.7 – 3.1 GHz, 2.9 – 3.1 GHz, 2.9 – 3.3 GHz and 3.1 – 3.5 GHz. The RF bipolar junction transistor (BJT) has been the workhorse technology used in these applications for its excellent performance, reliability and simple circuit design [1]. Lately there have been newcomers to this market space with both LDMOS and GaN HEMT technologies offering very competitive solutions in each frequency band. LDMOS is a mature technology due to its decade long use in wireless infrastructure applications, with an excellent reliability track record [2]. GaN HEMT, being a relatively newer technology, is less proven in the field, but thanks to its intrinsic advantages in terms of power density and bandwidth, has quickly gained a lot of attention, especially where bandwidth is a key requirement and performance differentiator. As a matter of fact, GaN HEMT technology enables a single device solution covering the entire radar bandwidth from 2.7 to 3.5 GHz, as in the 2-stage 75W GaN/SiC MMIC part supplied by Cree Inc. [3]. On the other hand, no LDMOS technology has been proven yet to achieve acceptable performance for radar transmitter application across a similar bandwidth and at comparable power levels.

In the present paper we introduce for the first time a high power LDMOS transistor technology for 2.7 – 3.5 GHz broadband radar applications. This enabling technology will offer a single solution for radars covering both the commercial and military application space. The excellent reliability and ruggedness under pulsed conditions (3:1 VSWR output mismatch and excellent immunity to problems stemming from parasitic bipolar action) of this internally matched LDMOS technology rely on its all gold metallization and gold bond wires [4]. In fact, Al wires should not be used in pulsed applications to avoid fatigue due to the continual flexing of the Al wire with each pulse which leads to embrittlement and eventual failure, and therefore using Au metallization intrinsically translates into a more reliable technology. To achieve excellent performance at S-band, the LDMOS transistor also features sub-micron gate length coupled with a grounded Faraday shield to isolate the gate from the drain and therefore reduce the feedback capacitance Cdg, as shown in the drawing of Fig. 1.

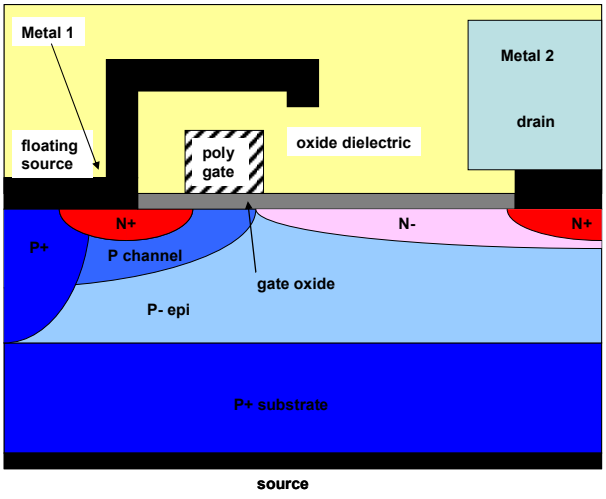


Fig. 1 Cross-section of an LDMOS design with Faraday Shield.

## II. RESULTS AND DISCUSSIONS

Two single-ended LDMOS transistors are housed in a push-pull style ceramic package. Each transistor is hybrid combined on the test fixture, i.e. the two halves of the push-pull transistor are connected in parallel on the test fixture PCB, which is shown in Fig. 2. The test fixture is matched to 50 ohms across the entire 2.7 - 3.5 GHz band.

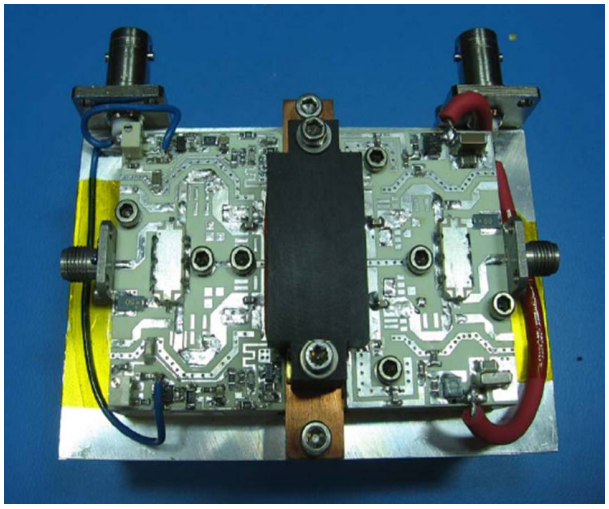

Fig. 2 Picture of 50Ω-matched test fixture for 130W LDMOS amplifier in 2.7 – 3.5 GHz broadband radar applications.

Four dice are used for each cavity of the dual-cavity package, for a total of 8 dice used in this part, as seen in Fig. 3.

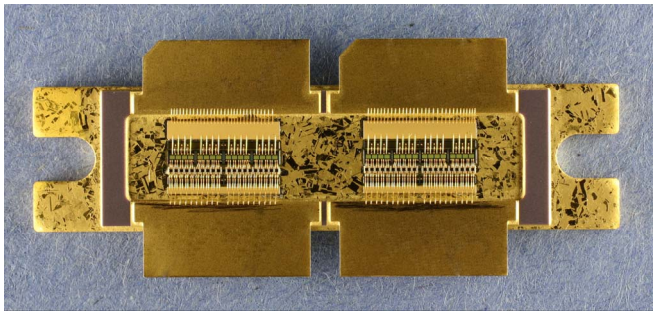

Fig. 3 130W LDMOS for 2.7 – 3.5 GHz broadband radar applications in push-pull style ceramic package.

The amplifier consists in a single-stage design with internal match to raise impedance to a manageable level for broadband matching through the fixture circuit. The part is internally matched at both input and output. The output match uses standard shunt L-C with series L matching network topology. In traditional narrow band applications the input match consists only of capacitors and inductors (bond wires) for standard L-C-L type T-networks. In broadband applications the use of series gate resistors allows easier input matching across an 800 MHz band. Utilizing matching networks with only capacitors and inductors to raise the low input impedance at the die to a higher level outside the package yields an impedance variation which is difficult to match using external microstrip matching networks. Therefore in our part the input match includes gate resistors to achieve broadband performance at the expense of some gain. The overall input match topology is an L-R-L-C-L network. With resistors added between the active device and the first section of impedance transformation, the bandwidth of the input match is improved. For the 2.7-3.5GHz S-band radar device developed, adding the input resistor improved the bandwidth of the input return loss by reducing the "Q" of the input matching structure[1]. The resistor is realized as a resistor array of many small resistor cells on a thin film substrate to provide good RF performance, and to distribute the resistance uniformly across the many transistor chips paralleled together. A close-up view of one of the package cavities showing the dice and the gate resistors is shown in Fig. 4.

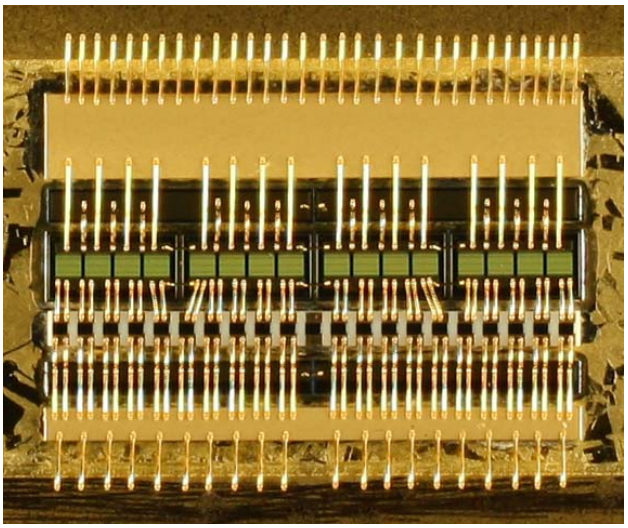

Fig. 4 Close-up view of one of the package cavities showing details of the dice and the gate resistors used for the input match.

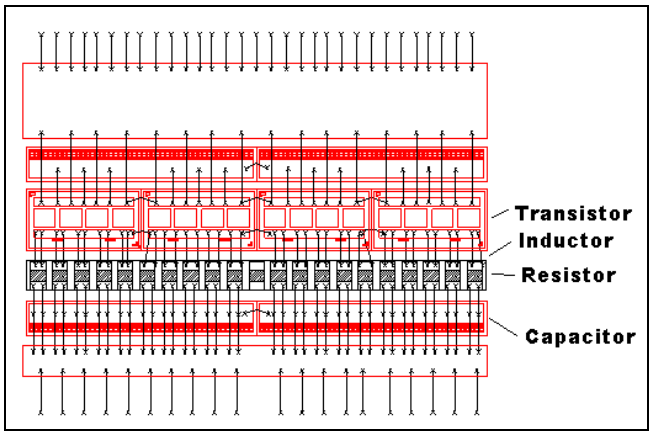


Fig. 5 Schematic view of one of the package cavities identifying the transistor cells, the series chip resistors, the shunt capacitors and the bonding wires.

[1] Patent pending

In Fig. 5 a schematic illustrating the wire bonding scheme with the location and identification of the transistors, resistors and capacitors is shown. Each transistor side consists of 4 active cells with a small isolation gap between them for excellent thermal performance. Five chip resistors are used for each die, for a total of 20 chip resistors used in the input match in each cavity of the package. An extra dummy resistor is visible between the two pairs of dice, but it is unused. Each chip resistor has 1.5Ω resistance. In Fig. 6 the plot of the impedance contours across the 2.7-3.5 GHz band are compared with and without the addition of input gate resistors. The plots compare a model of the S-band LDMOS transistor input impedance at the lead reference plane, with (red) and without (green) the added input resistor. The contours clearly show how the addition of the resistors reduces the impedance variation, thus facilitating the design and realization of a test fixture matching topology across the band. Measured data of the input return loss for one cavity only are reported in Table 1.

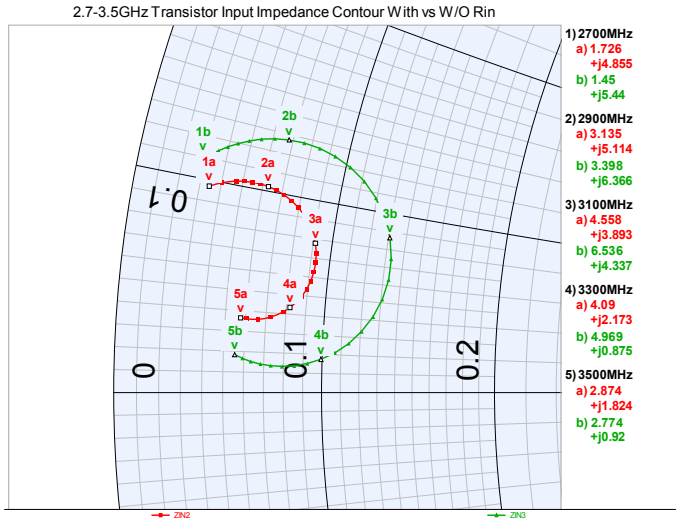


Fig. 6 Input impedance contours for the 2.7 – 3.5 GHz S-band LDMOS transistor with the input resistors (red) versus without them (green).

Table 1

| Freq [GHz] | 2.7 | 2.9 | 3.1 | 3.3 | 3.5 |
|---|---|---|---|---|---|
| IRL [dB] | -6 | -18 | -11 | -10 | -11 |

Measured IRL data across the 2.7 – 3.5 GHz band for one cavity of the package.

The transistor is typically biased in class AB at a drain voltage of 32V and 20mA quiescent current, i.e. the device draws 20mA in the absence of any applied pulse. This virtually pure class B bias maximises efficiency at the expense of RF gain. Another possibility for pulse operation that would yield high gain and high efficiency simultaneously would be with over-lapping DC & RF pulses with a higher quiescent current. However, this bias condition has not been explored at the present time and therefore the following pulsed RF data refer to a bias condition which does not include gate bias modulation. With a signal pulse of 300us and 10% duty cycle, the part supplies a minimum output power of 130W across the band, although P1dB ranges from 135W to 170W at each frequency. Typical measured RF data are shown in Figs. 7 – 9.

As shown in Fig. 7, the pulse droop never exceeds -0.3dB across the band reflecting the excellent thermal properties of the LDMOS transistor for pulsed applications. Die thickness is 3 mils.

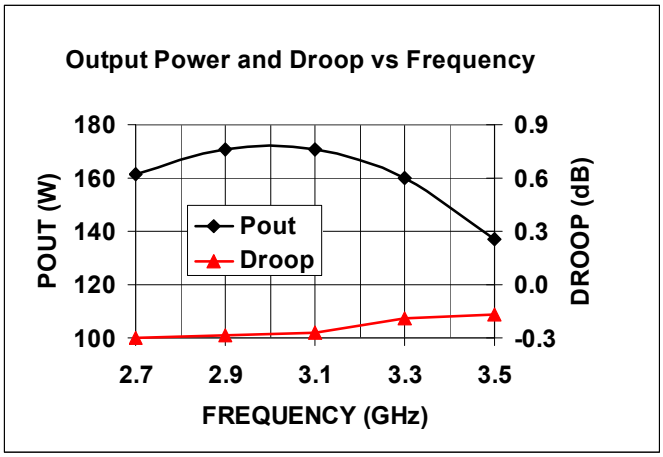


Fig. 7 Output power at P1dB and droop during the pulse vs. frequency for the LDMOS transistor biased at 20mA and 32V. Signal pulse condition is 300us and 10% duty cycle.

In Fig. 8 we report the input return loss across the band showing excellent matching conditions at all frequencies. Unlike the IRL data reported in Table 1, this input return loss data is measured at the input of the hybrid combined part, i.e. it accounts for matching of both cavities of the package. The power gain exceeds a minimum of 8dB, which is enough for most output stage designs in radar transmitters [5]. Although 8dB gain seems low compared to competing GaN technologies, it is worth remembering that this LDMOS part is based on a single-stage amplifier design, compared with 2 gain stages in the GaN MMIC, so 8dB gain is sufficient for the output stage.

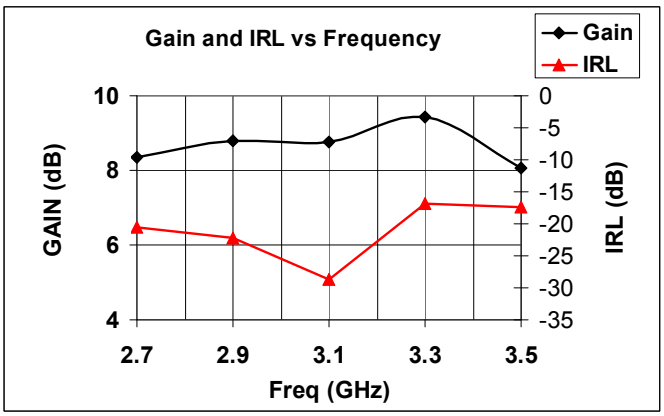


Fig. 8 Power gain and input return loss (IRL) vs. frequency for the LDMOS transistor biased at 20mA and 32V. Signal pulse condition is 300us and 10% duty cycle.

Next, in Fig. 9 we show the drain efficiency across the band, which is relatively constant in the range of 36% to 38%. This is relatively low, when theoretically it should be 78%, but because in this applications there is a 25% BW, it is impossible to present the optimum load impedance to the FET at any point in the band.

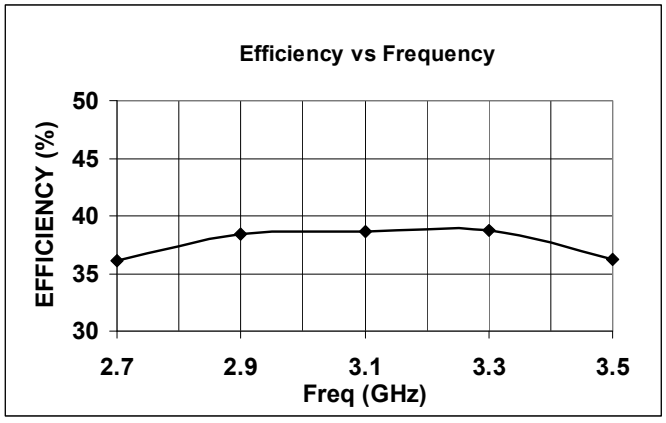


Fig. 9 Drain efficiency vs. frequency for the LDMOS transistor biased at 20mA and 32V. Signal pulse condition is 300us and 10% duty cycle.

From a thermal and reliability standpoint the transistor is well suited for pulsed operation in the field. Gold metallization and gold bond wires assure no purple plague or poor electro-migration related failures. Each of the 8 dice used in the part has a thermal resistance of 1.28 °C/W under CW operation. The part consisting of 8 chips has a thermal resistance of 0.16 °C/W. With a nominal output power of 120W (pulsed operation) the part draws 11.26A of average DC current. Biased at 32V the input DC power is 360W, which translates into a dissipated power of 240W. Therefore, the junction temperature rise is 0.16 °C/W x 240W = 38.4 °C above the case temperature, which is 85 °C, with a total junction temperature of 123.4 °C below the safe threshold of 125 °C. The reader should also keep in mind that operation is pulsed with pulses of 300us and 10% duty cycle. Therefore the above estimated junction temperature of 123.4 °C is reached at the end of the 300us pulse, and the average temperature would actually be much closer to the case temperature of 85 °C for extra safety margins and better reliability. A similar die used in the part described in this paper is also used in other S-band transistor parts for standard frequency bands from 2.7 to 3.1 GHz and from 3.1 to 3.5 GHz. Some of these parts have gone through RF burn-in without any reported failure. Overall the authors have accumulated over 20 month operation of parts using the same die without any incident. The junction temperature calculation outlined above confirms the part would operate well within accepted junction temperature limits for reliable operation in the field.

Ruggedness is relatively good, passing the 3:1 VSWR load mismatch at a rated power of 120W. For comparison, it is also noteworthy that the BJT (Bipolar Junction Transistor) technology traditionally used for such radar applications, has al least three disadvantages to the LDMOS technology described in this paper: LMT (load mismatch tolerance), Stability into VSWR and Bandwidth. In these three respects there basically is no comparison between the two technologies. For instance, silicon BJTs at these frequencies and bandwidths are tested to withstand only a 2:1 load mismatch tolerance (LMT). LDMOS can easily withstand an LMT of 3:1. For stability, silicon BJTs are tested to pass 1.5:1 VSWR with 1dB input overdrive. This is more reflective of the final module environment in which parts do work. But the LDMOS transistor is completely stable into 3:1 and probably even more. Finally, BJT can only cover and is tested in the more traditional radar bandwidths (2.7-3.1GHz or 3.1-3.5GHz) and not the entire 2.7 – 3.5 GHz frequency range. Our LDMOS design, on the other hand, has shown better ruggedness measures at higher power levels and larger bandwidth. It is reasonable to expect that with future enhancements to the die design higher power levels, with similar or better gain and efficiency figures across the 2.7 – 3.5 GHz band are also achievable.

## III. CONCLUSIONS

An LDMOS technology for 2.7 – 3.5 GHz broadband radar applications covering both commercial and military markets has been introduced for the first time. The die features an all gold metallization for ultimate reliability in radar pulsed applications. The high power discrete transistor is internally matched, also using gold bond wires, over the 2.7 - 3.5 GHz frequency range and the broadband text fixture is matched to 50 Ω requiring no external tuners. Biased at 32V in class AB, with a 300us and 10% duty cycle pulse signal, the single-ended transistor achieves a minimum of 130W with 8dB gain and 36% drain efficiency across the 800 MHz band. The authors believe that Integra's groundbreaking 2.7 – 3.5 GHz LDMOS solution is a valid alternative to more expensive competing technologies such as GaN HEMT.

## ACKNOWLEDGMENT

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