

**60W L-Band Radar LDMOS**

The high power transistor part number ILD1214M60 is designed for the frequency band 1215-1400 MHz. Operating 3at 300us-10% pulse conditions this LDMOS FET device supplies a minimum of 60 watts of power across the instantaneous operating bandwidth of 1215-1400 MHz. All devices are 100% screened for large signal RF parameters.



**Silicon LDMOS FET**

- High Power Gain
- Superior thermal stability

**Class AB Operation**

- Gate biased to  $I_{DQ} = 550 \text{ mA}$

**Configuration**

- Common Source

**Gold Metal**

- Maximum Reliability

**Package**

- Thermally enhanced
- Pb-free and RoHS-compliant

**Epoxy Sealed Lid**

- Gross Leak Qualified

**RF Test Fixture**

- Broadband
- Matched to  $50\Omega$
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning required

**TYPICAL DATA      TYPICAL DATA      TYPICAL DATA      TYPICAL DATA**

General Information ILD1214M60	Test Sequence Name	Freq (MHz)	PIN (W)	RL (dB)	POUT (W)	GP (dB)	dG (dB)	Id (A)	nd (%)	Droop (dB)	VSWR-LMT 3:1	VSWR-LMT 3:1 (P-F)
Date: 5/6/2009												
Assbly Lot - SN : D3792-3	Nominal	1215	3	-18.0	78	14.15		9.490	65.2	0.11	P	P
Wafer : NA												
Test Fixture : NA	Nominal	1300	3	-17.0	68	13.55	0.73	9.400	58.1	0.06	P	P
Pass / Fail : Device Passes												
OPERATOR: FB	Nominal	1400	3	-15.0	66	13.42		9.250	58.7	0.03	P	P
Vd=30V Idq=550mA												

**MAXIMUM RATINGS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Drain-Source Voltage	$V_{DSS}$	--	65	V	--
BD	Gate-Source Voltage	$V_{GS}$	-0.5	12	V	--
BD	Storage Temperature Range	$T_{STG}$	-40	+150	°C	--
BD	Operating Junction Temperature Range	$T_J$	-55	+200	°C	--
Note	Screen 'BD' = parameter qualified By Design.					

**THERMAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	TBD	°C/W	$V_{DS}=30V, I_{DQ}=50mA, T_F=25\pm 5^\circ C, P_{IN}=3W, 300us/10\%$ .
Note	Screen 'BD' = parameter qualified By Design.					

**PROCESSING SPECIFICATIONS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

**DC ELECTRICAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Drain-Source Breakdown Voltage	$BV_{DSS}$	65	--	V	$I_D = 10mA, V_{GS} = 0V, T_F = 25\pm 5^\circ C$
100%	Drain Leakage Current	$I_{DSS}$	--	2	$\mu A$	$V_{DS} = 30V, V_{GS} = 0V, T_F = 25\pm 5^\circ C$
100%	Gate Threshold Voltage	$V_{GSTH}$	2.0	4.0	V	$I_{DQ} = 100mA, V_{DS} = 5V, T_F = 25\pm 5^\circ C$
100%	Gate Leakage Current	$I_{GSS}$	--	1	$\mu A$	$V_{GS} = 5V, V_{DS} = 0V, T_F = 25\pm 5^\circ C$

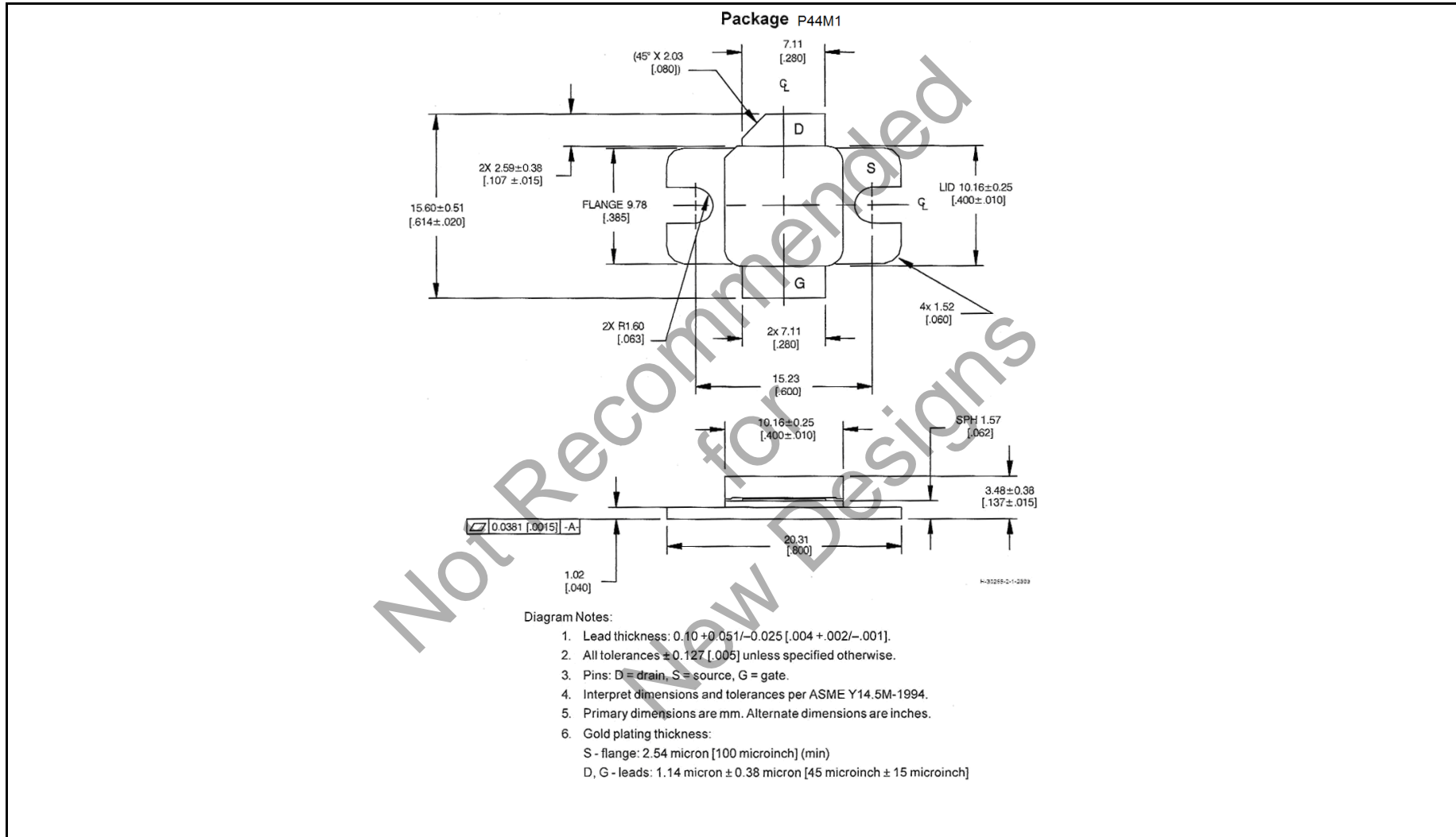
**RF ELECTRICAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	RL	-18	-10	dB	$V_d=30V, P_{IN} = 3W, 300us/10\%, I_{dq}=50mA, T_F=25\pm 5^\circ C, F=F1, F2, F3.$
100%	Power Gain	$G_p$	13.0	15.0	dB	$V_d=30V, P_{IN} = 3W, 300us/10\%, I_{dq}=50mA, T_F=25\pm 5^\circ C, F=F1, F2, F3.$
100%	Output Power	$P_{out}$	60	95	W	$V_d=30V, P_{IN} = 3W, 300us/10\%, I_{dq}=50mA, T_F=25\pm 5^\circ C, F=F1, F2, F3.$
100%	Drain Efficiency	$N_d$	42	75	%	$V_d=30V, P_{IN} = 3W, 300us/10\%, I_{dq}=50mA, T_F=25\pm 5^\circ C, F=F1, F2, F3.$
100%	Load Mismatch Tolerance	VSWR-LMT	3:1	--	--	$V_d=30V, P_{IN} = 3W, 300us/10\%, I_{dq}=50mA, T_F=25\pm 5^\circ C, F=F1, F2, F3,$ Rotate 3:1 output VSWR through 360° phase. Survival.
100%	Gain Flatness	GF	0	2	dB	$V_d=30V, P_{IN} = 3W, 300us/10\%, I_{dq}=50mA, T_F=25\pm 5^\circ C, F=F1, F2, F3.$
100%	Signal Amplitude Droop	Droop	-0.5	0.5	dB	$V_d=30V, P_{IN} = 3W, 300us/10\%, I_{dq}=50mA, T_F=25\pm 5^\circ C, F=F1, F2, F3.$
Note 1	F1= 1215 MHz, F2= 1300 MHz, F3= 1400 MHz.					
Note 2	$T_F$ = Device flange temperature.					
Note 3	Screen 'BD' = parameter qualified By Design.					

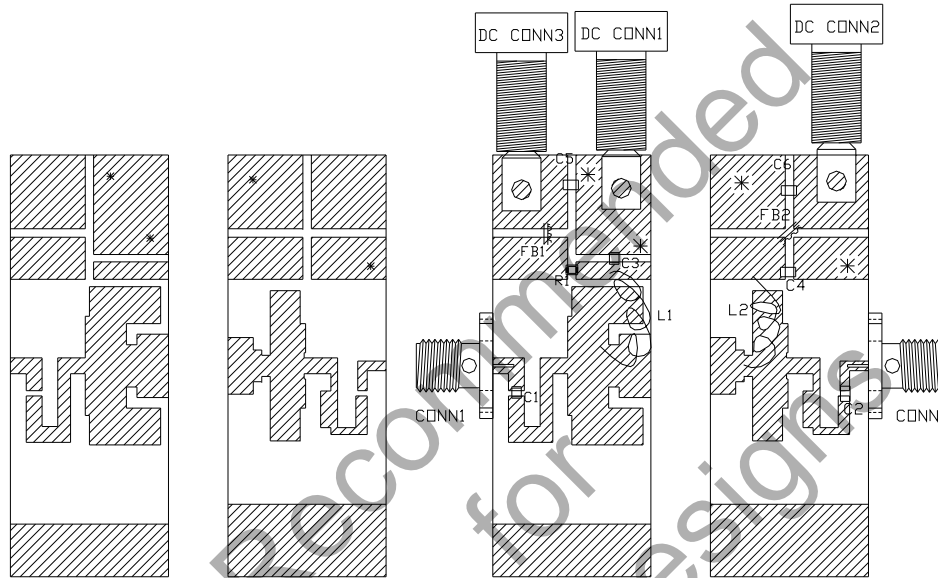
**RF TEST FIXTURE IMPEDANCE CHARACTERISTICS**

Frequency (MHz)	$Z_{IF} (\Omega)$	$Z_{OF} (\Omega)$
1215	2.83 - j0.32	4.03 - j1.20
1300	2.49 - j0.38	3.97 - j1.00
1400	1.91 - j0.13	3.69 - j0.82

**PACKAGE DIMENSIONAL OUTLINE DRAWING**

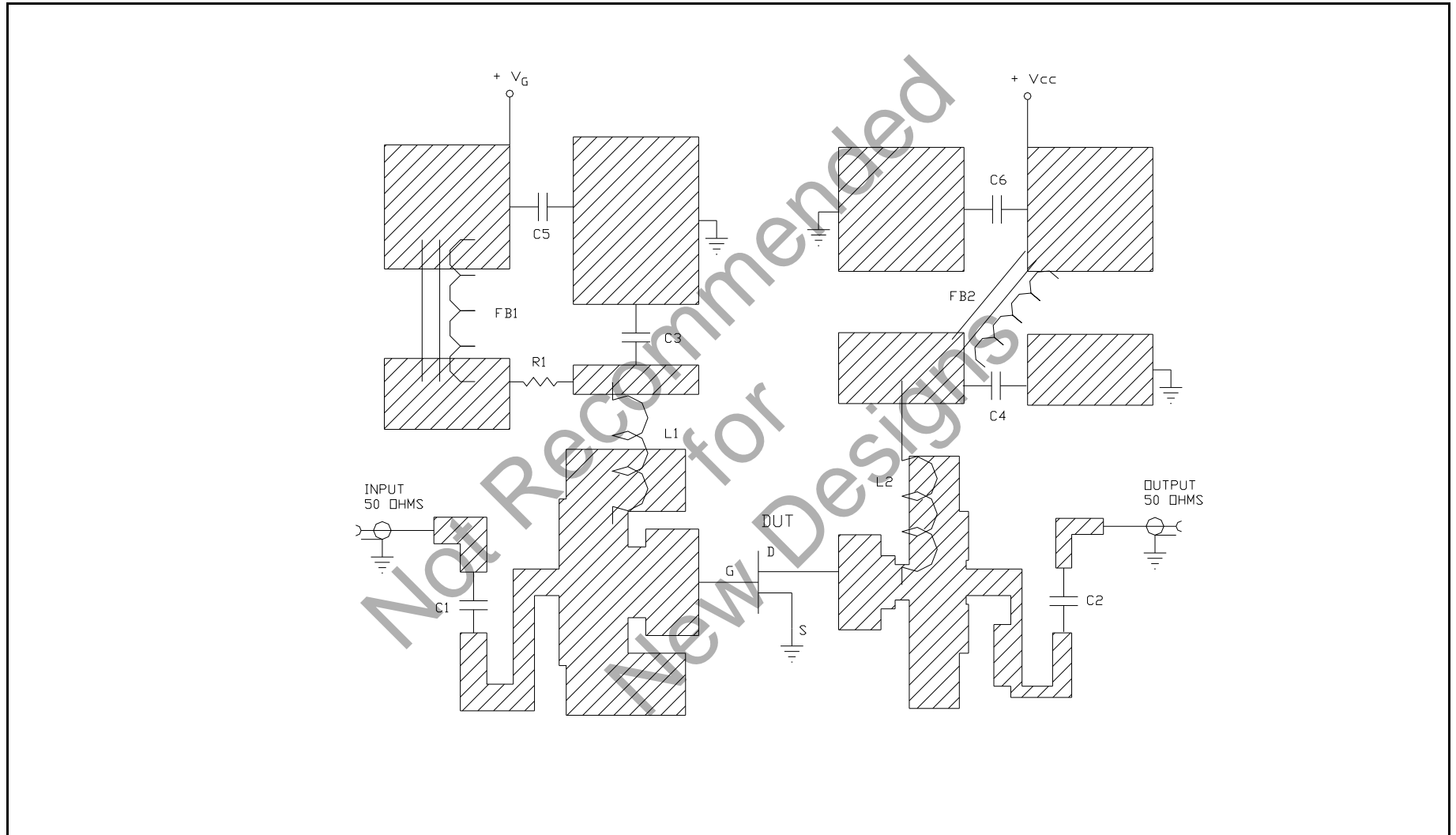


**RF TEST FIXTURE – ASSEMBLY AND PARTS LIST**

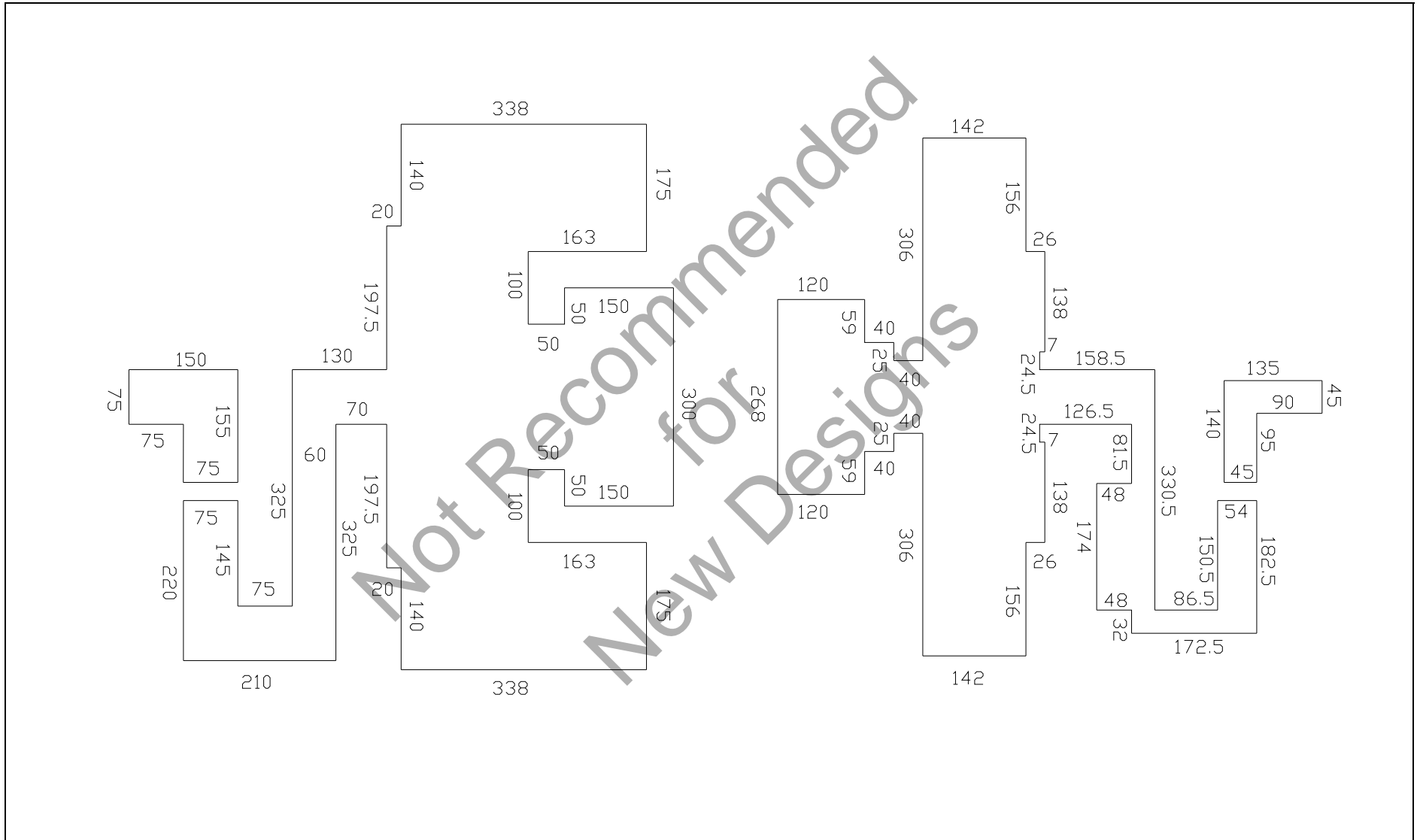


COMPONENT	DESCRIPTION
DUT	TRANSISTOR #ILD1214M60, MOUNT HARD TO THE RIGHT
PC BOARD	ROGERS RT6010, 2LM 1oz. Cu, BOTH SIDES
C1, C2, C3, C4	CHIP CAPACITOR, 33 pF
C5	CHIP CAPACITOR, 3300 pF
C6	CHIP CAPACITOR, 1uF
GS	GROUND SHIM, COPPER, TH=0.001" *
CONN1, CONN2	SMA CONNECTOR, TYPE DS #2052-5636-02
INPUT PC BOARD CARRIER	2 INCH BRASS - 02
OUTPUT PC BOARD CARRIER	2 INCH BRASS - 02
TRANSISTOR CARRIER	2 INCH COPPER - 15
TRANSISTOR CLAMP	NORYL CLAMP -15
HEATSINK	2 INCH HEATSINK - 11
DC CONN1	BANANA JACK, BLACK
DC CONN2	BANANA JACK, RED
DC CONN3	BANANA JACK, BLUE
FB1, FB2	FERRITE BEAD
R1	CHIP RESISTOR, 10 ohms
L1, L2	INDUCTOR, 6 TURNS, WIRE# 22, ID= 0.100"
NOTE	FIXTURE HARDWARE DRAWINGS AVAILABLE ON REQUEST

**RF TEST FIXTURE – ELECTRICAL SCHEMATIC**



**RF TEST FIXTURE – CIRCUIT DIMENSIONS IN MILS**



**DEFINITIONS**

<b>Data Sheet Status</b>	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
<b>Maximum Ratings</b>	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only. Operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

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Not Recommended for New Designs