

# X-Band, GaN/SiC, RF Power Transistor

8.9 - 9.4 GHz | 80 W | 43% Efficiency | 12 dB Gain | 50 V | 200µs Pulse Length, 10% Duty Cycle

IGT8994M50 is a high power GaN-on-SiC RF power transistor that has been designed to suit the unique needs of X-Band Radar Systems. It operates over the full bandwidth of 8.9-9.4 GHz. Under 200µs, 10% duty cycle pulse conditions, it supplies 50 W of peak output power, with an associated 10 dB of gain and 38% efficiency. It operates from a 50 V supply voltage. For optimal thermal efficiency, the transistor is housed in a metal-based package with an epoxy-sealed ceramic lid.



## FEATURES

- GaN on SiC HEMT Technology
- Output Power >50 W
- Fully matched to 50 Ω Impedance at both Input and Output
- High Efficiency - up to 43%
- 100% RF Tested
- RoHS and REACH Compliant

## APPLICATIONS

- X-band Radar Systems

BLOCK DIAGRAM

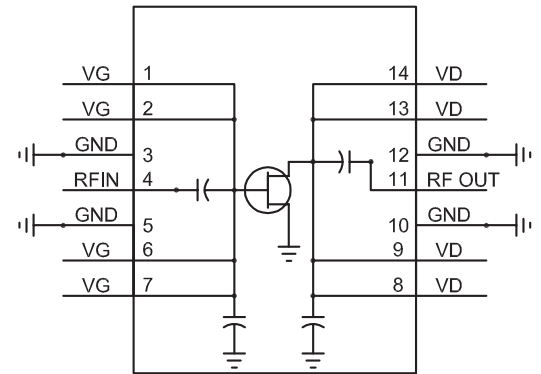


Table 1. Absolute Maximum Ratings (Not Simultaneous)

Parameter	Symbol	Value	Units	Test Conditions
DC Drain-Source Voltage	$V_{DS}$	130	V	25 °C
DC Gate-Source Voltage	$V_{GS}$	-8 to +1.0	V	25 °C
DC Drain Current	$I_D$	4.8	A	25 °C
DC Gate Current	$I_G$	1	mA	25 °C
RF Input Power	$P_{RFIN}$	8	W	25 °C
Operating Junction Temperature	$T_J$	-55 to +200	°C	
Storage Temperature	$T_{STG}$	-55 to +150	°C	
Soldering Temperature	$T_{SOLDER}$	260 for 10s	°C	

Note: Operation outside the limits given in this table may cause permanent damage to the transistor

Table 2. DC Electrical Characteristics (Case temperature = 25 °C unless otherwise stated)

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Gate Pinch-Off Voltage	$V_P$	-5.0			V	$V_{DS} = 50V, I_{DS} = 1mA$
Quiescent Gate Voltage	$V_Q$		-2.6		V	$V_{DS} = 50V, I_{DS} = 10mA$

**Table 3. RF Electrical Characteristics (Case temperature = 30 °C unless otherwise stated)**

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Input Return Loss	IRL	18	10	5	dB	$P_{OUT} = 50W$ $f = 8.9, 9.15, 9.4 \text{ GHz}$ 200µs on, 10% $V_{DS} = 50V, I_{DS} = 10mA,$
Gain	G		10		dB	
Drain Efficiency	$\eta$		38		%	
Pulse Droop	D		-0.5		dB	
Load Mismatch Stability	VSWR-S	2:1				
VSWR Withstand	VSWR-LMT	3:1				

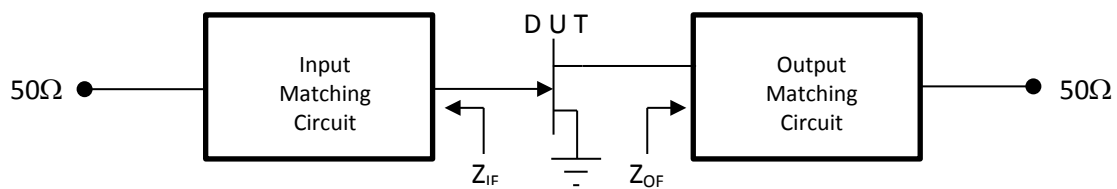
Note: Consult Integra Technologies Application Note 001 for information on how RF output power and pulse droop are measured.

**Table 4. Thermal Resistance (Case temperature = 25 °C unless otherwise stated)**

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Peak Thermal Resistance, Junction to Case	$R_{TH(JC)}$				°C/W	$P_{OUT} = 50W$ $f = 9.15 \text{ GHz}$ 200µs on, 10% $V_{DS} = 50V, I_{DS} = 10mA$

**Table 5. Optimum Source & Load Impedances (Case temperature = 25 °C unless otherwise stated)**

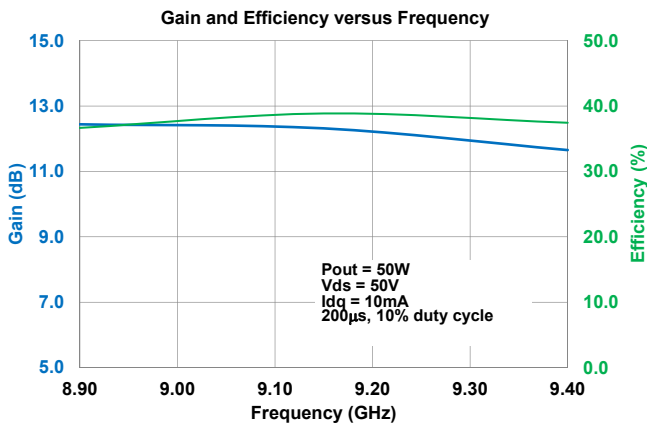
Frequency (GHz)	$Z_{IF}$	$Z_{OF}$	Units	Test Conditions
8.9	50 + j0	50 + j0	$\Omega$	$P_{OUT} = 50W$ 200µs pulse length, 10% duty cycle $V_{DS} = 50V, I_{DS} = 10mA$
9.15	50 + j0	50 + j0	$\Omega$	
9.4	50 + j0	50 + j0	$\Omega$	



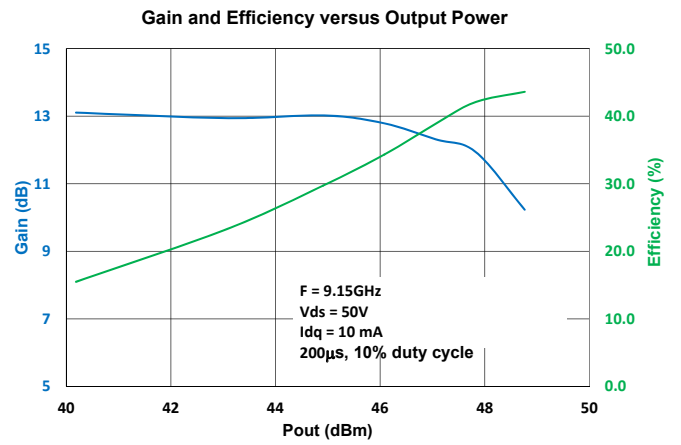
**DC Bias Sequencing**

TURN ON SEQUENCE	TURN OFF SEQUENCE
<ol style="list-style-type: none"> <li>1. Turn RF Power OFF</li> <li>2. Set <math>V_{GS} = -5V</math> (Negative Voltage to pinch off FET)</li> <li>3. Measure <math>I_{DS}</math> current, should be &lt;1mA.</li> <li>4. Turn ON <math>V_{DS}</math> voltage.</li> <li>5. Slowly increase <math>V_{GS}</math> until bias current reaches <math>I_{DQ}</math>.</li> <li>6. Turn ON RF Power</li> </ol>	<ol style="list-style-type: none"> <li>1. Turn OFF RF Power</li> <li>2. Turn OFF <math>V_{DS}</math> voltage</li> <li>3. After <math>V_{DS}</math> is discharged, set <math>V_{GS} = -5V</math></li> <li>4. Turn OFF <math>V_{GS}</math> voltage.</li> </ol>

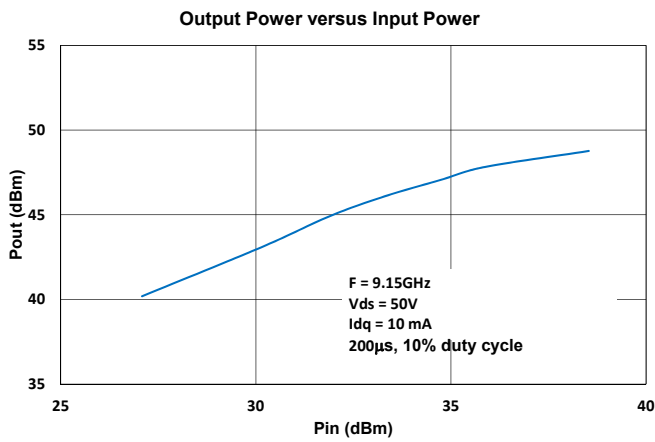
**TYPICAL PERFORMANCE**



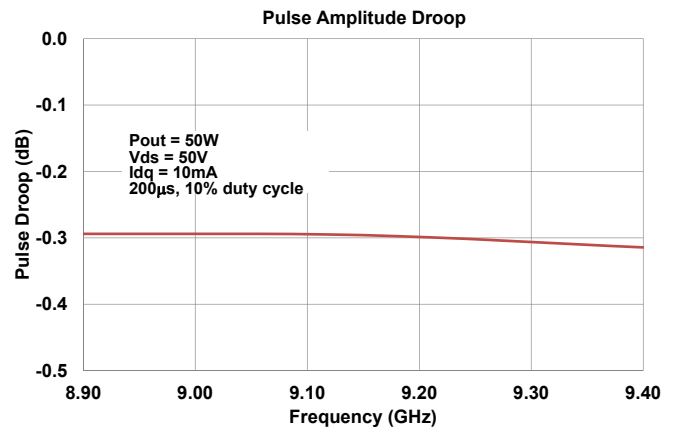
**Figure 1**



**Figure 2**

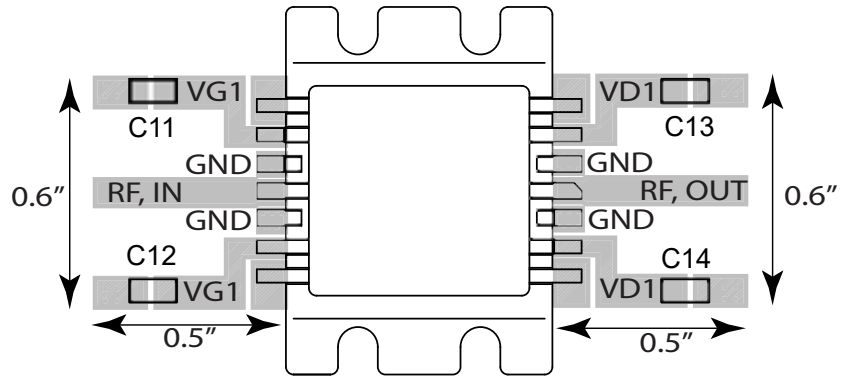


**Figure 3**

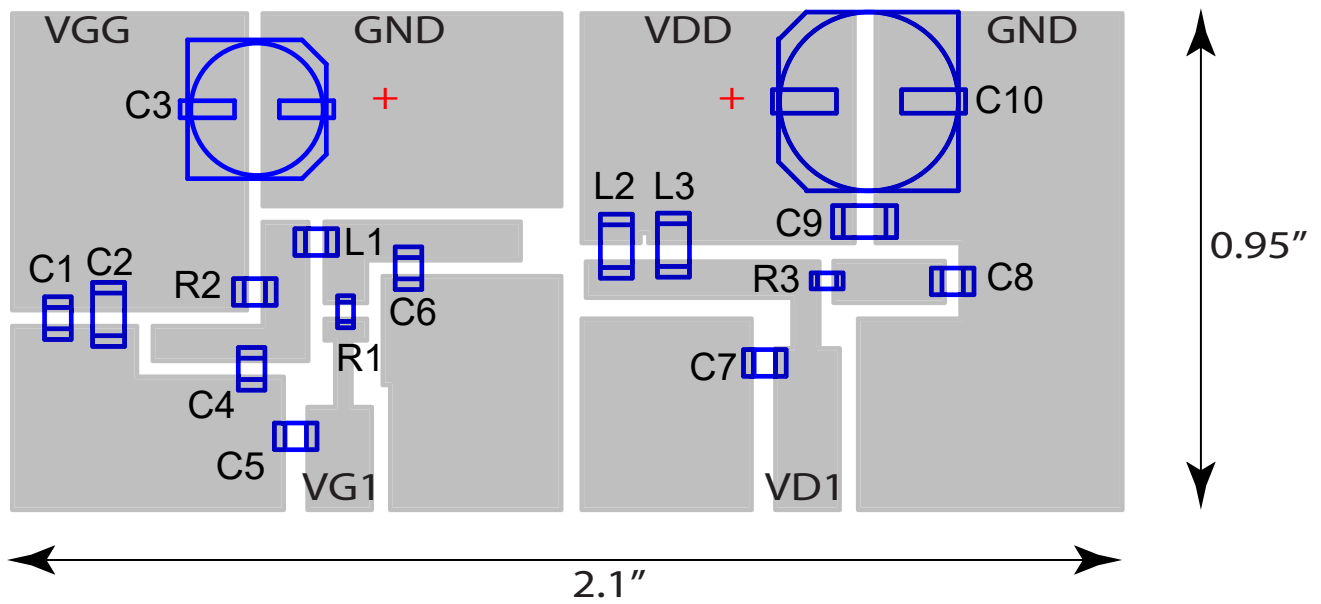


**Figure 4**

**RF BOARD**



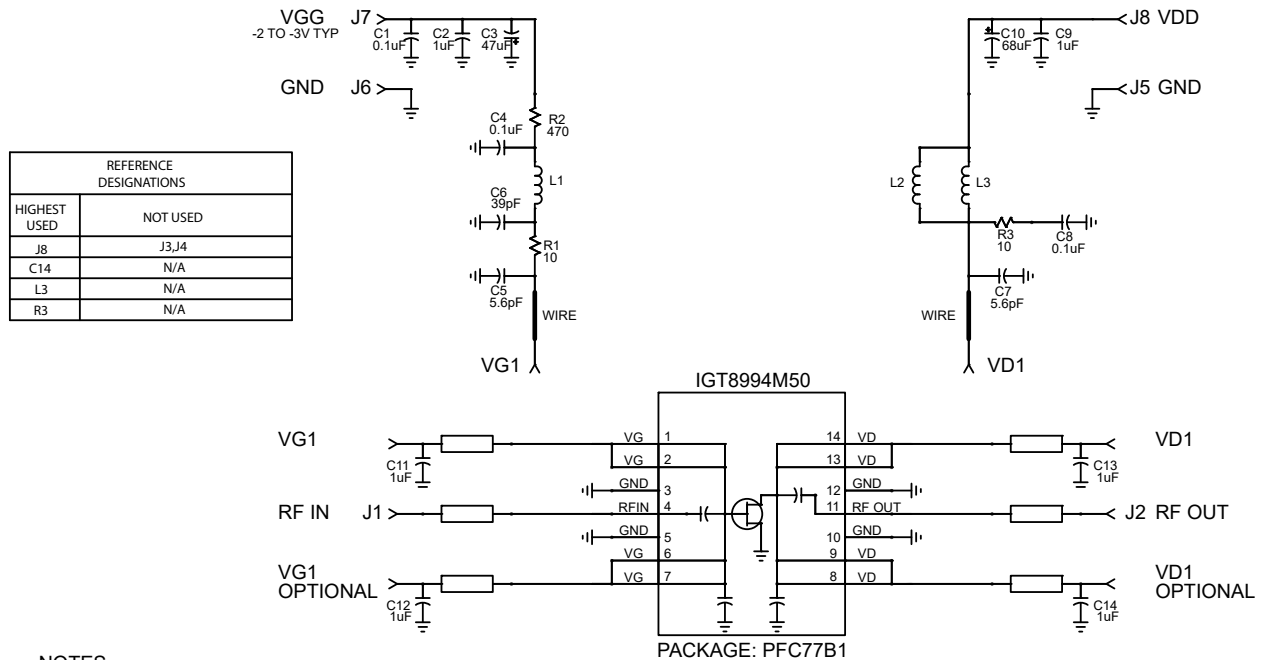
**BIAS BOARD**



**Bill of Materials for IGT8994M50 Test Fixture**

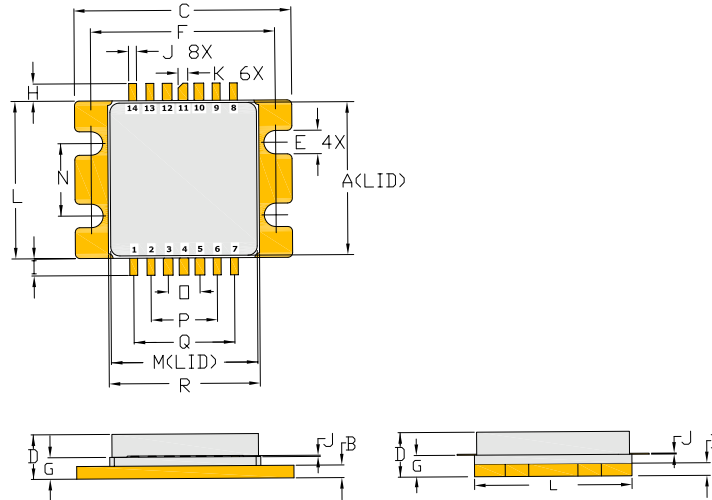
Designator	Description	Part Number
C1, C4, C8	CAP 0.1 $\mu$ F, 0805, 100V	C0805C104K1RAL
C2, C9, C11, C12, C13, C14	CAP 1 $\mu$ F, 1206, 100V, X7R	GRM31CR72A105KA01L
C3	CAP 47 $\mu$ F, 25V, 20% SMT	PCV1E470MCL2GS
C5, C7	CAP 5.6pF, 0805, +/-0.25, 250V, EDGE MOUNT	ATC600F5R6CT
C6	CAP 39pF, 0805, 250V	ATC600F390
C10	CAP Electrolytic, 68 $\mu$ F, 20%, 63V, SMD	EEE-FK1J680P
L1	IND, FB, 120 OHM, 0805, 5A	ILHB0805ER121V
L2, L3	IND, FB, 33 OHM 100MHz, 1206, 6A	BLM31PG330S
R1, R3	RES, 10 OHM, 0603	
R2	RES, 470 OHM, 0805	
RF Board Type	TACONIC RF-35TC-0300-C1/C1, DK=3.5, 0.03" thick, 1/1oz, Copper	
Bias Board Type	ROGERS RO4350B-0300-0.5ED/0.5ED, DK=3.5, 0.03" thick	

**IGT8994M50 CIRCUIT SCHEMATIC**



- NOTES**
- 1) PINS 1,2,6,7 CONNECTED INTERNALLY.
  - 2) PINS 8,9,13,14 CONNECTED INTERNALLY.
  - 3) VG CAN BE BIASED FROM EITHER PINS 1 & 2 OR PINS 6 & 7.
  - 4) VD CAN BE BIASED FROM EITHER PINS 8 & 9 OR PINS 13 & 14.
  - 5) RF PINS 4 AND 11 ARE BOTH INTERNALLY DC DECOUPLED.
  - 6) THERE SHOULD BE GROUND PADS WITH VIAS ON THE PCB FOR PINS 3,5,10,&12.

**PACKAGE PFC77B1**



DIM	INCHES		MILLIMETER	
	MIN	MAX	MIN	MAX
A	0.660	0.670	16.76	17.02
B	0.051	0.059	1.30	1.50
C	0.941	0.949	23.90	24.10
D	0.192	0.215	4.88	5.46
E	0.098	0.106	2.49	2.69
F	0.799	0.807	20.29	20.50
G	0.090	0.098	2.29	2.49
H	0.071	0.079	1.80	2.01
I	0.071	0.079	1.80	2.01
J	0.030	0.038	0.76	0.97
K	0.038	0.046	0.97	1.17
L	0.681	0.689	17.30	17.50
M	0.632	0.642	16.05	16.31
N	0.311	0.319	7.90	8.10
P	0.134	0.142	3.40	3.61
P	0.284	0.292	7.21	7.42
Q	0.434	0.442	11.02	11.23
R	0.653	0.661	16.59	16.79

### ESD & MSL Rating

Parameter	Rating	Standard
ESD Human Body Model (HBM)	TBD	ESDA/JEDEC JS-001-2012
ESD Charged Device Model (CDM)	TBD	JEDEC JESD22-C101F
Moisture Sensitivity Level (MSL)	Unlimited Shelf Life	IPC/JEDEC J-STD-020

### RoHS Compliance

Integra Technologies, Inc declares that its GaN and LDMOS Transistor Products comply with EU Directive 2011/65/EU on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS2), as adopted by EU member states on January 2, 2013 and amended on March 31, 2015 by EU Directive 2015/863/EU.

### REACH Compliance

Integra Technologies supports EU Regulation number 1907/2006 concerning the Registration, Evaluation, Authorization, and Restriction of Chemicals (REACH) as these apply to Integra semiconductor products, development tools, and shipping packaging.

In support of the REACH regulation, Integra will:

- Inform customers and recipients of Integra product if they contain any substances that are of very high concern (SVHC) per the European Chemical Agency (ECHA) website.
- Notify ECHA if any Integra product that contains any SVHCs which exceed guidelines for REACH chemicals by weight per part number and for total content weight per year for all products produced in or imported to the European market.
- Cease shipments of product containing REACH Annex XIV substances until authorization has been obtained.
- Cease shipment of product containing REACH Annex XVII chemicals when restrictions apply.

Integra has evaluated its materials, BOMs, and product specifications and product and has determined that this transistor conforms to all REACH and SVHC regulations and guidelines. Integra has implemented actions and control programs that will assure continued compliance.

### Disclaimer

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**DEFINITIONS:**

**DATA SHEET STATUS**

Advanced Specification - This data sheet contains Advanced specifications.

Preliminary Specification - This data sheet contains specifications based on preliminary measurements and data.

Final Specification - This data sheet contains final product specifications.

**MAXIMUM RATINGS** Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.

Integra Technologies, 321 Coral Circle, El Segundo, CA 90245-4620 | Phone: 310-606-0855 | Fax: 310-606-0865