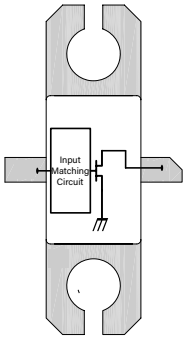
L-Band, GaN/SiC, RF Power Transistor

960 - 1220 MHz | 110W typ | 55% Efficiency typ | 17dB Gain typ | 100 V | 32μs Pulse Length, 4% Duty Cycle

IGN0912S110HV and IGN0912S110HVS are high power GaN-on-SiC RF power transistors that have been designed to suit the unique needs of IFF and TACAN/DME systems. They operate over the full 960 - 1220 MHz frequency range. Under 32μs, 4% duty cycle pulse conditions, they supply a minimum of 110 W of peak output power. They operate from a 100V supply voltage. For optimal thermal efficiency, the transistors are housed in a metal-based package with an epoxy-sealed ceramic lid.

FEATURES

- GaN on SiC HEMT Technology
- Output Power >110W
- Pre-matched Input Impedance
- High Efficiency - 55% typical
- 100% RF Tested Under 32μs, 4% duty cycle pulse conditions
- RoHS and REACH Compliant



APPLICATIONS

- IFF and TACAN/DME Systems

Table 1. RF Electrical Characteristics in Broadband Test Fixture (Case temperature = 30 °C unless otherwise stated)

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Gain	G	15	17.5	19	dB	P_{OUT} = 110W
Drain Efficiency	η	45	55	65	%	f = 960, 1090, 1220 MHz
Pulse Droop	D	-0.3	-0.15	+0.1	dB	32μs pulse length, 4% duty cycle
Load Mismatch Stability	VSWR-S		2:1			V_{DS} = 100V, I_{DS} = 8mA
VSWR Withstand	VSWR-LMT		5:1			

Note: Consult Integra Technologies Application Note 001 for information on how RF output power and pulse droop are measured.

Table 2. Absolute Maximum Ratings (Not Simultaneous)

Parameter	Symbol	Value	Units	Test Conditions
DC Drain-Source Voltage	V_{DS}	200	V	25 °C
DC Gate-Source Voltage	V_{GS}	-8 to +1.0	V	25 °C
DC Drain Current	I_D	2	A	25 °C
DC Gate Current	I_G	2	mA	25 °C
RF Input Power	$P_{RF,IN}$	5	W	25 °C
Operating Channel Temperature	T_{CH}	-55 to +225	°C	
Storage Temperature	T_{STG}	-62 to +150	°C	
Soldering Temperature	T_{SOLDER}	260 for 60s	°C	

Note: Operation outside the limits given in this table may cause permanent damage to the transistor

Table 3. DC Electrical Characteristics (Case temperature = 25 °C unless otherwise stated)

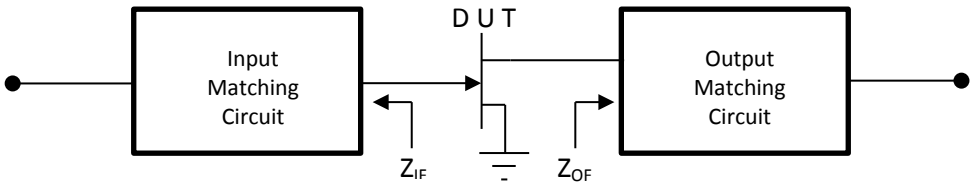
Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Gate Pinch-Off Voltage	V_P	-5.0			V	V_{DS} = 100V, I_{DS} = 1mA
Quiescent Gate Voltage	V_Q		-2.8		V	V_{DS} = 100V, I_{DS} = 8mA

Table 4. Thermal Resistance (Case temperature = 85 °C unless otherwise stated)

Parameter	Symbol	Typ	Units	Test Conditions
Peak Thermal Resistance, Channel to Case	R_{TH}	1.6	°C/W	P_{DISS} =90W 32µs pulse length, 4% duty cycle V_{DS} = 100V

Table 5. Test Fixture Source & Load Impedances

Frequency (MHz)	Z_{IF}	Z_{OF}	Units	Test Conditions
960	7.13 - j 2.47	13.29 + j 16.78	Ω	P_{OUT} = 110W 32µs pulse length, 4% duty cycle V_{DS} = 100V, I_{DS} = 8mA
1090	7.04 + j 0.19	17.49 + j 16.27	Ω	
1220	7.62 + j 2.81	20.60 + j 14.71	Ω	



TYPICAL PERFORMANCE

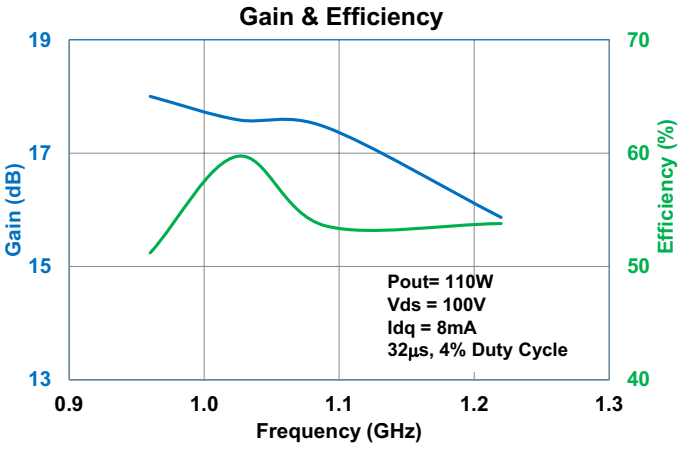


Figure 1

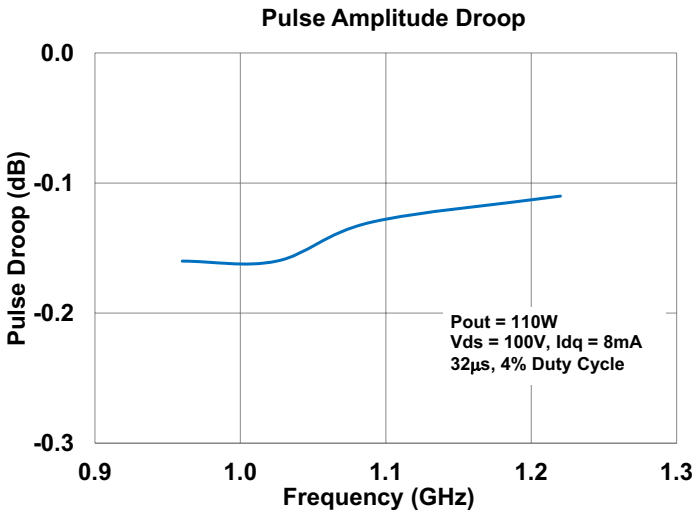


Figure 2

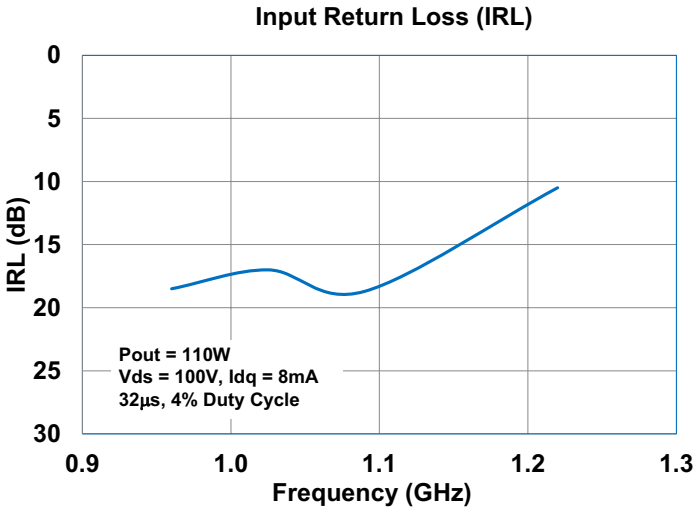
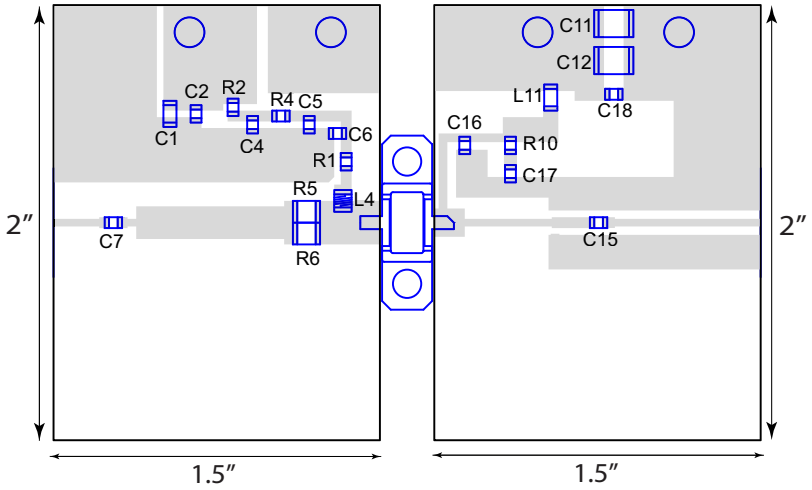


Figure 3

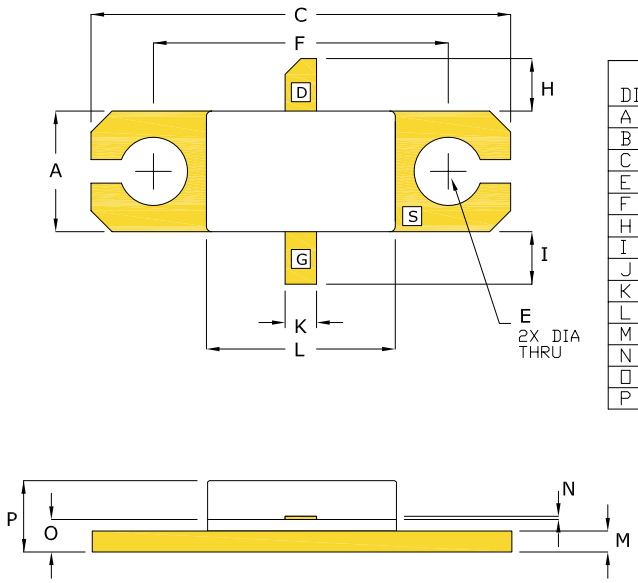
TEST FIXTURE



Bill of Materials for IGN0912S110HV Test Fixture

Designator	Description	Quantity	Part Number
C1	CAP 1 µF, 100V, 1206, X7R	1	12061C105K4T2A
C2, C5, C18	CAP 1000pF, 100V, 0805	3	08051A102J4T2A
C4, C17	CAP 0.068µF, 250V, 0805, X7R	2	C0805C683KARAC#A
C6, C7, C16	CAP 33pF, 0805	3	600F330FT250XT
C11, C12	CAP 1µF, 200V, 1812, X7R	2	18122C105KAT2A
C15	CAP 18pF, 0805	1	600F180JT250XT
L4	IND 39nH, 1008	1	1008CS-390XJLB
L11	IND FB 1206, 6A, 33 OHM	1	BLM31PG330SN1L
R1, R10	RES 5.1 OHM, 0805	2	CRCW08055R1JNEA
R2	RES 200 OHM, 0805	1	CRCW0805200RFKTA
R4	RES 0 OHM, 0805	1	CRCW08050000ZSTA
R5, R6	RES 2 OHM, 1210	2	CRCW12102R00JNEA
PC Board Type	ROGERS RO3006, 25mil, 1/1oz. Copper	2	

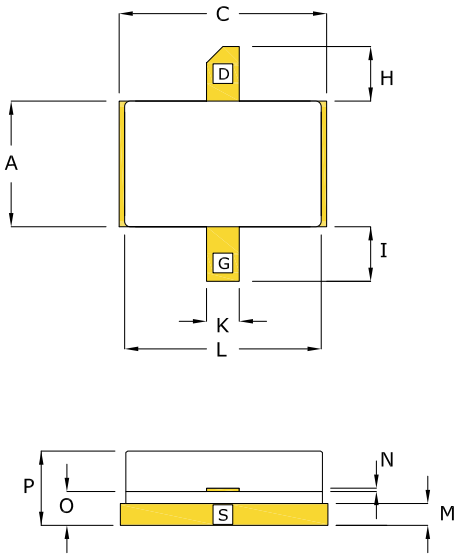
PACKAGE PL32C2



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.225	0.235	5.72	5.97
B	--	--	--	--
C	0.795	0.805	20.19	20.44
E	0.125	0.135	3.18	3.43
F	0.557	0.567	14.14	14.40
H	0.090	0.110	2.29	2.79
I	0.090	0.110	2.29	2.79
J	--	--	--	--
K	0.055	0.065	1.40	1.65
L	0.357	0.363	9.07	9.22
M	0.035	0.045	0.89	1.14
N	0.004	0.006	0.10	0.15
O	0.057	0.067	1.45	1.70
P	0.131	0.154	3.33	3.91

PIN SCHEDULE	
D	DRAIN
S	SOURCE
G	GATE

BOLT-DOWN FLANGE OPTION
IGN0912S110HV



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.225	0.235	5.72	5.97
B	--	--	--	--
C	0.375	0.385	9.53	9.78
E	--	--	--	--
F	--	--	--	--
H	0.090	0.110	2.29	2.79
I	0.090	0.110	2.29	2.79
J	--	--	--	--
K	0.055	0.065	1.40	1.65
L	0.357	0.363	9.07	9.22
M	0.035	0.045	0.89	1.14
N	0.004	0.006	0.10	0.15
O	0.057	0.067	1.45	1.70
P	0.131	0.154	3.33	3.91

PIN SCHEDULE	
D	DRAIN
S	SOURCE
G	GATE

EARLESS FLANGE OPTION
IGN0912S110HVS

ESD & MSL Rating

Parameter	Rating	Standard
ESD Human Body Model (HBM)	TBD	ESDA/JEDEC JS-001-2012
ESD Charged Device Model (CDM)	TBD	JEDEC JESD22-C101F
Moisture Sensitivty Level (MSL)	Unlimited Shelf Life	IPC/JEDEC J-STD-020

RoHS Compliance

Integra Technologies, Inc declares that its GaN and LDMOS Transistor Products comply with EU Directive 2011/65/EU on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS2), as adopted by EU member states on January 2, 2013 and amended on March 31, 2015 by EU Directive 2015/863/EU.

REACH Compliance

Integra Technologies supports EU Regulation number 1907/2006 concerning the Registration, Evaluation, Authorization, and Restriction of Chemicals (REACH) as these apply to Integra semiconductor products, development tools, and shipping packaging.

In support of the REACH regulation, Integra will:

- Inform customers and recipients of Integra product if they contain any substances that are of very high concern (SVHC) per the European Chemical Agency (ECHA) website.
- Notify ECHA if any Integra product that contains any SVHCs which exceed guidelines for REACH chemicals by weight per part number and for total content weight per year for all products produced in or imported to the European market.
- Cease shipments of product containing REACH Annex XIV substances until authorization has been obtained.
- Cease shipment of product containing REACH Annex XVII chemicals when restrictions apply.

Integra has evaluated its materials, BOMs, and product specifications and product and has determined that this transistor conforms to all REACH and SVHC regulations and guidelines. Integra has implemented actions and control programs that will assure continued compliance.

Disclaimer

Integra Technologies Inc. reserves the right to make changes without further notice to any products herein. Integra Technologies Inc. makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Integra Technologies Inc. assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. Integra Technologies Inc. products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Integra Technologies Inc. customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Integra Technologies Inc. for any damages resulting from such improper use or sale.

DEFINITIONS:
DATA SHEET STATUS
Advanced Specification - This data sheet contains Advanced specifications.
Preliminary Specification - This data sheet contains specifications based on preliminary measurements and data.
Final Specification - This data sheet contains final product specifications.
MAXIMUM RATINGS Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.

Integra Technologies, 321 Coral Circle, El Segundo, CA 90245-4620 | Phone: 310-606-0855 | Fax: 310-606-0865