

# Analysis of a GaN/SiC UHF Radar Amplifier for Operation at 125V Bias

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**Abstract**—The relationship between Fe concentration in the buffer layer and breakdown voltage of an AlGaIn/GaN on SiC HEMT transistor has been investigated to achieve operation of the device in a UHF power amplifier operated at a bias of 100V or higher. A 15mm transistor has been tested in a power amplifier at the frequency of 430MHz with a 100 $\mu$ s pulse and 10% duty factor, operated at 75V, 100V, 125V and 150V bias. At 100V bias, the device achieves 250W output power and 78% drain efficiency with 27dB gain almost independently of Fe content; at 125V bias, only the devices with Fe content above 1e18 cm<sup>-3</sup> achieve a saturated power in excess of 350W with 75% drain efficiency and 27dB gain. RF burn-in tests indicate very stable operation. To the authors' knowledge, this is the first time that UHF pulsed radar amplifier operation has been reported at voltages above 100V with GaN technology.

**Keywords**—amplifier, breakdown voltage, Fe doping, buffer layer, UHF, 125V bias.

## I. INTRODUCTION

High breakdown voltage in AlGaIn/GaN HEMT transistors is a desirable feature that enables high voltage blocking capability in power management applications and high bias operation in RF amplifiers. Although there is an ongoing research effort to achieve high breakdown voltage for stable high voltage switching applications, much less attention is devoted to high power amplifiers in GaN technology operated at 100V bias or higher. Such a technology could be used in high power amplifiers for applications in UHF weather radar, long-range tracking radar, ISM applications or as vacuum tubes replacement in radar systems. For instance, there are available silicon devices, such as the bipolar junction transistor and both the vertical and lateral diffused MOS field effect transistors which can operate at 100V bias at VHF, or the silicon carbide static induction transistor which has lower than 10dB gain and barely 50% efficiency at only 450MHz and therefore it has never really been accepted in the marketplace. In this work the advantages that GaN technology offers when operated, for example, at 125V bias are explored. The chosen frequency is 430MHz which is well above where 100V silicon technology operates.

It has been shown by several authors that Fe incorporation in the buffer layer of an AlGaIn/GaN HEMT device helps achieve higher breakdown voltage, especially when using a Silicon substrate [1]. Intentional Fe doping in the GaN channel region of the device also helps mitigate short-channel effects, as shown by the authors in reference [2]. A retrograde profile

is typically used, with peak Fe concentration close to the AlN nucleation layer and carrier substrate (SiC, Si or sapphire), having a gradual or linear decline towards the surface, resulting in a Fe-free GaN channel region close to the interface with the AlGaIn barrier, or the AlN spacer between the GaN channel and the AlGaIn barrier layers whenever the AlN layer is used in the epi structure. A typical range of Fe concentration in the buffer is from 2e17 cm<sup>-3</sup> to 3e18 cm<sup>-3</sup>. Lower concentrations are less effective in compensating the slightly n-type buffer layer resulting from the un-intentional incorporation of Si atoms during MOCVD growth. Much higher peak Fe concentration results in too high trap density, leading to current collapse and related effects. Fe doped buffer layer also results in increased piezoelectric induced tensile stress at the AlGaIn/GaN interface, but it has also been demonstrated that lateral electric field during transistor operation results in self-heating with a very sharp non-uniform temperature profile, which results in compressive thermal strain/stress [3], and the tensile and compressive strains are of the same order of magnitude thus partially offsetting each other. Unlike Fe doping, which can be controlled relatively well, Carbon (C) is a common contaminant in MOCVD growth which is much harder to control and is more dependent on the reactor design and the process parameters used during growth, as recently reported in reference [4]. C creates very deep-level acceptor traps (~0.9eV from the conduction band) that have been demonstrated to generate much larger current-collapse effects [5]. On the other hand, Fe creates trap levels located much closer to the GaN conduction band (0.5eV deep) and it only has minor contributions to DC-RF dispersion or current collapse [5]. Because of this, C level in the buffer layer, especially in the GaN channel region close to the interface with the AlGaIn barrier, tends to be kept as low as possible, preferably below 1e17 cm<sup>-3</sup> [4].

In this work the peak Fe concentration in the buffer layer has been varied from 5e17 cm<sup>-3</sup> to 1e18 cm<sup>-3</sup> and 3e18 cm<sup>-3</sup> and drain-source breakdown voltage has been measured. Additionally, design parameters of the AlGaIn/GaN HEMT device were also varied in terms of drift region and source field plate length. Drain-source breakdown voltage greater than 600V has been achieved with the combination of higher Fe concentration and longer drift region. A large size (15mm gate periphery) GaN HEMT transistor has been utilized in a power amplifier operated at 75V, 100V, 125V and 150V bias as a vehicle to understand the device stability and reliability under high bias operation. RF tests at 430MHz were done under pulse conditions with 100 $\mu$ s pulse width and 10% duty cycle. Results

show stable operation at most bias and Fe level configurations. To the authors knowledge such results are the first of its kind.

## II. BREAKDOWN VOLTAGE ENHANCEMENT TECHNIQUES

### A. Epi Structure and Transistor Layout

The GaN HEMT on SiC technology used for our research utilizes an epi structure consisting of: a low temperature AlN nucleation layer, a GaN channel and a buffer layer Fe-doped away from the channel region with a thickness ranging from 1.5 $\mu\text{m}$  - 2 $\mu\text{m}$ , the AlGaN barrier, and a 3nm thick GaN cap. Several wafers were grown with a different level of Fe peak concentration in the buffer; namely, 5e17  $\text{cm}^{-3}$ , 1e18  $\text{cm}^{-3}$  and 3e18  $\text{cm}^{-3}$ . Sheet resistance is in the 360 – 390  $\Omega/\square$  range. C concentration was kept uniform, being 1e17  $\text{cm}^{-3}$  or lower. A typical Fe and C profile is shown for reference in Figure 1.

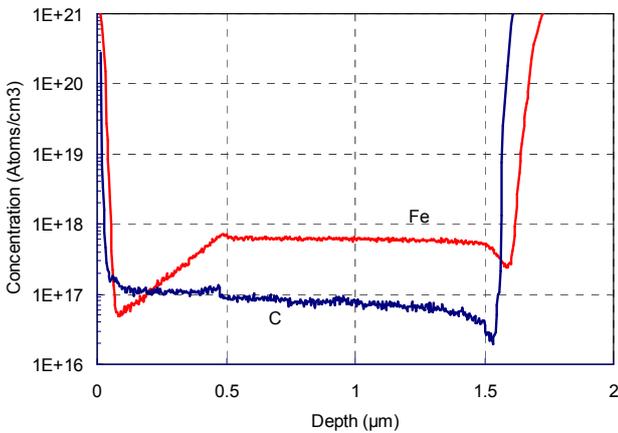


Fig. 1. Typical Fe and C profiles in the buffer layer of a GaN HEMT.

Transistor parameters were varied to optimize the device; namely, the source field plate and the drift region length. The combinations were: 4.15 $\mu\text{m}$ , 6.65 $\mu\text{m}$  and 9.15 $\mu\text{m}$  drift region length with a field plate extension about half the drift region length. Gate length of the chips is 1 $\mu\text{m}$ . The large chips with 9.15 $\mu\text{m}$  drift region have 15mm total gate periphery. In this paper the focus of the research work for RF operation is on these 15mm devices with 9.15 $\mu\text{m}$  drift region.

### B. GaN HEMT Process Flow

The AlGaIn/GaN HEMT transistors are built on the well-established and mature fabrication process flow from Integra Technologies, Inc. Ohmic contacts are made of a Ti/Al/Ni/Au metal stack, annealed in a short and high-temperature RTP step. A triple ion-implantation step is used for device isolation. Surface passivation, which is a very critical step for obtaining DC-RF dispersion-free GaN transistors, is accomplished by PECVD low-stress silicon nitride deposition. For this project a 1 $\mu\text{m}$  gate length shallow trench is then formed by a low-damage silicon nitride etch step, followed by a 0.5 $\mu\text{m}$  thick Ni/Au gate metal stack e-beam deposition that forms a 0.5 $\mu\text{m}$  gate overhangs for the gate-connected field plate. Another

silicon nitride deposition step is used for isolation between the gate field plate and the next source connected field plate. The second field plate layer is formed with another e-beam Au-based metal layer that also adds metal on top of the source and drain ohmic contacts for lower contact resistance. The final steps of the front-side process include the formation of air bridges through plated Au. Wafer processing is completed after back-grinding the SiC substrate to a 3 to 4-mil thickness. No back-via process is used on the wafers for the experiments reported in the present paper. The die is attached to the package flange with AuSn pre-form at 320  $^{\circ}\text{C}$  and the source pads are connected to the package flange through Au bond wires.

## III. DC RESULTS

The 3-terminal breakdown voltage at 1mA/mm drain-source current was measured on unit cells of the chips described above. The gate-source junction is reverse-biased at -5V. Results indicate that  $BV_{DSS}$  does increase with an increase in peak Fe concentration in the buffer, as shown in Figure 2.

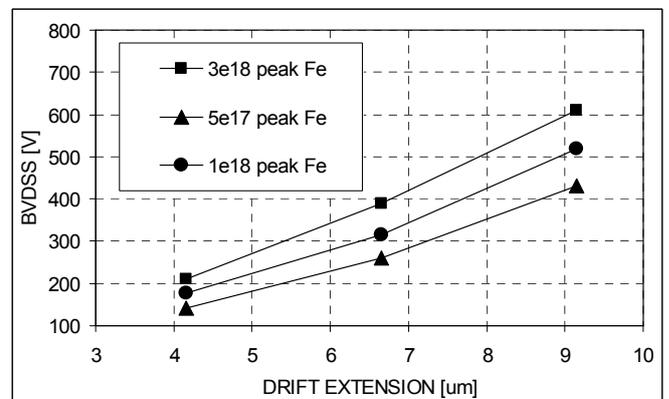


Fig. 2. BVDSS vs. drift region length and peak Fe concentration in the buffer layer of a GaN HEMT.

The drift region extension is the most sensitive parameter for achieving higher breakdown voltage. However, BVDSS increases from 140V to 210V with 4.15 $\mu\text{m}$  drift extension when increasing the peak Fe concentration in the buffer layer from 5e17 to 3e18  $\text{cm}^{-3}$ . With 6.65 $\mu\text{m}$  drift region the increase is from 260V to 390V; with the longer drift region of 9.15 $\mu\text{m}$  the breakdown voltage increases from 430V to 610V. With  $BV_{DSS}$  ranging from 430V to 610V, the transistor topology featuring the 9.15 $\mu\text{m}$  gate-drain extension is definitely suitable for operation up to 150V in a typical class E power amplifier, where the maximum drain-source voltage swing is typically up to  $\sim 3.5\times$  the bias voltage  $V_{DD}$ .

## IV. RF RESULTS

In our approach a mixed-mode circuit topology based on a combination of class E and inverse class F has been used, as reported in [6]. The same baseline test fixture has been used in all cases; in each measurement the device was matched for maximum output power with external slug tuners at 0.1W input power and then driven harder while keeping the same tuning. A cooling fan ensured the test fixture was kept at a temperature of 35  $^{\circ}\text{C}$ . Three samples of the 15mm total gate periphery die with

9.15 $\mu\text{m}$  drift region extension were assembled into a ceramic package and tested in a power amplifier at the frequency of 430MHz. Each sample is from a wafer with  $5\text{e}17\text{ cm}^{-3}$ ,  $1\text{e}18\text{ cm}^{-3}$  and  $3\text{e}18\text{ cm}^{-3}$  peak Fe concentration. RF data were collected on output power, drain efficiency and power gain. Each transistor is operated successively at 75V, 100V, 125V and 150V bias with a pulsed signal of 100 $\mu\text{s}$  length and 10% duty cycle. Using a pulsed signal helps keep the thermal effects negligible. Power gain and drain efficiency versus output power are presented in Figures 3, 4, 5 and 6 for the 75V, 100V, 125V and 150V bias condition, respectively.

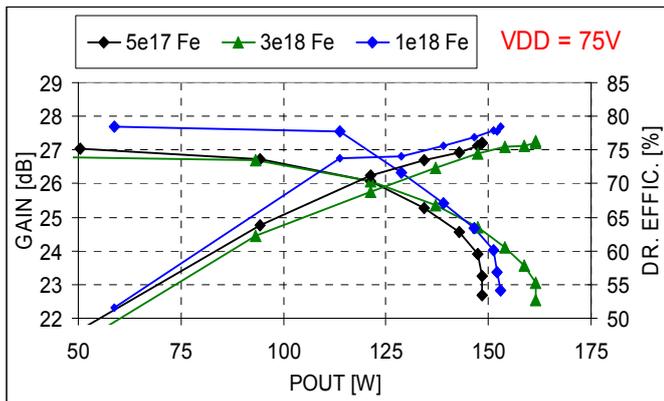


Fig. 3. Gain and drain efficiency vs. output power drive-up at 430MHz for the 75V bias condition. Pulse length is 100 $\mu\text{s}$  and duty factor is 10%.

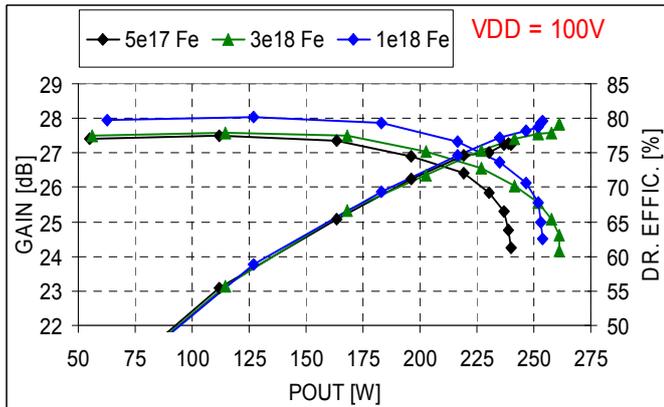


Fig. 4. Gain and drain efficiency vs. output power drive-up at 430MHz for the 100V bias condition. Pulse length is 100 $\mu\text{s}$  and duty factor is 10%.

RF data for the three device families are roughly identical at 75V and 100V bias, as illustrated in Figures 3 and 4, with the variations more likely due to slight differences in tuning and to measurement errors. On the contrary, a well defined difference in maximum output power and drain efficiency is observed at 125V and 150V bias, as illustrated in Figures 5 and 6. The sample with peak Fe concentration of  $5\text{e}17\text{ cm}^{-3}$  tolerates very well operation up to 100V bias with saturated output power increasing from  $\sim 150\text{W}$  to  $\sim 240\text{W}$  when bias increases from 75V to 100V, just like for the samples with higher Fe content. When the bias is further increased to 125V and 150V, the

saturated power increases only marginally to  $\sim 300\text{W}$  and  $\sim 325\text{W}$  respectively for the sample with  $5\text{e}17\text{ cm}^{-3}$  peak Fe concentration, whereas saturated output power increases to  $\sim 350\text{W}$  and  $\sim 425\text{W}$  on the samples with  $1\text{e}18\text{ cm}^{-3}$  and  $3\text{e}18\text{ cm}^{-3}$  peak Fe concentration. Further to this analysis, the sample with  $3\text{e}18\text{ cm}^{-3}$  Fe content seems to be slightly better than the one with  $1\text{e}18\text{ cm}^{-3}$  Fe. The next piece of information we gather from the measured data is the trend observed in power gain and drain efficiency versus bias. Looking at Figures 3, 4, 5 and 6 the linear gain seems to stay relatively constant in the 27dB - 28dB level over the bias range from 75V to 150V. On the other hand, the maximum drain efficiency at saturated power seems to drop on average by 5% points at 150V, whereas it stays in the 75% - 80% range when the operating bias is 75V, 100V and 125V. A possible explanation is that the test fixture was optimized for the 100V, 250W operation point for best efficiency, which includes 2<sup>nd</sup> and 3<sup>rd</sup> harmonic tuning on the bias line of the test fixture, as reported in reference [6].

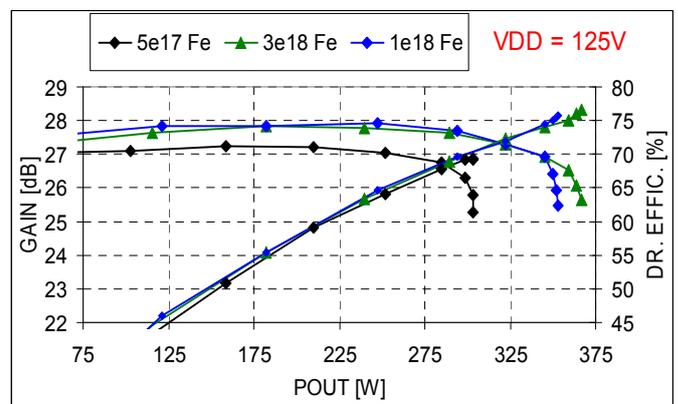


Fig. 5. Gain and drain efficiency vs. output power drive-up at 430MHz for the 125V bias condition. Pulse length is 100 $\mu\text{s}$  and duty factor is 10%.

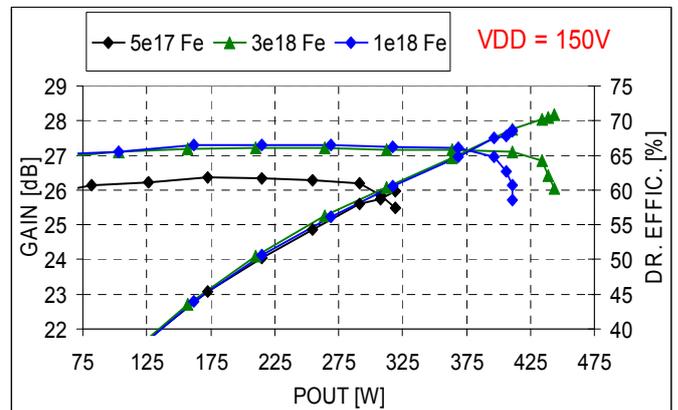


Fig. 6. Gain and drain efficiency vs. output power drive-up at 430MHz for the 150V bias condition. Pulse length is 100 $\mu\text{s}$  and duty factor is 10%.

Higher voltages and saturated power levels require a different output match for the fundamental and harmonics. As the operation voltage increases, the fundamental impedance also increases, reducing the amount of tuning or capacitance required at the fundamental. The lower capacitance degrades

the match at the harmonics, therefore eliminating optimum harmonic reflections back into the device. Nonetheless, with  $\sim 350\text{W}$  saturated power and 76% drain efficiency the 15mm device operated at 125V has an outstanding power density of 23W/mm. With a transistor operated at 125V and a power density of 23W/mm it is important to prove that the device is reliable enough to operate in the field with an acceptable lifetime. A preliminary reliability analysis has been conducted by doing 1-week RF burn-in at ambient temperature, with the test fixture under forced air cooling at a temperature of 26 °C. In Figure 7 we show variations of RF output power in percentage and gain reduction in dB at 125V for the three samples utilized in our work. Results show that degradation in power and gain after a week operation is relatively small; within 5%. Most of the degradation occurs during the first day. The most striking result is the fact that the samples with higher peak Fe concentration in the buffer layer exhibit lower degradation. The authors believe that further reduction of the output power drift at 125V could be achieved by further optimization of the epi structure and field plate design.

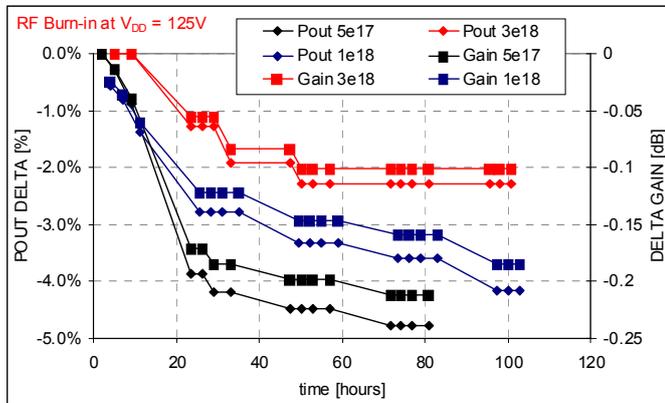


Fig. 7. Gain and output power variation at 125V during RF burn-in.

Based on the device layout, the junction temperature is calculated based on the nonlinear model discussed in [7] which has been shown to be very accurate. At 350W output power and 76% drain efficiency the peak drain current is 3.7A when the supply voltage is 125V; therefore the DC power is  $3.7\text{A} \times 125\text{V} = 460\text{W}$  (or  $350\text{W}/76\% = 460\text{W}$ ), and the dissipated power is  $460\text{W} - 350\text{W} = 110\text{W}$ . The model discussed in [7] has been extended to include the effect of the package, with an  $R_{\text{TH}}$  of 0.094 °C/W. For die attach we have used AuSn with 20um thickness, as the pre-form sheet is 1-mil thick. Its thermal resistance is 0.12 °C/W. Including the nonlinearity of the SiC substrate and GaN epi-layer ( $\sim 2\mu\text{m}$  thick) thermal conductivity, their calculated thermal resistances are 1.144 and 0.15 °C/W respectively. Therefore, the total thermal resistance is 1.51 °C/W. For a base-plate temperature of 26 °C under forced air cooling, the junction temperature with 110W dissipated power reaches a peak value of 192 °C which is acceptable for reliability in a wide band-gap material such as GaN. However, the model has been adapted to transient analysis under the 100μs pulse width and 10% duty cycle used in our tests.

Values for density and specific heat of the different material layers to calculate the thermal capacitance have been taken from reference [8], table 2. For a base-plate temperature of 26 °C under forced air cooling, the calculated peak channel temperature is only 126 °C which is excellent from a reliability standpoint considering the 125V technology with 23W/mm power density. A more stringent set of reliability tests ought to be carried out to better quantify the degradation of this device while in operation. Nonetheless the authors believe that the pioneering results reported in this paper demonstrate that an RF GaN amplifier for UHF radar pulsed operation at bias voltage of 125V is indeed possible at 430MHz.

## V. CONCLUSIONS

A UHF power amplifier has been analyzed with a GaN HEMT transistor designed to operate at bias voltages above the 100V mark. Acceptable RF performance with bias voltages ranging from 75V up to 150V has been demonstrated. The most important conclusion is that as the bias of operation is increased above 100V so must the Fe content in the buffer layer of the GaN device. From a quantitative analysis a buffer with peak Fe content above  $1e18\text{ cm}^{-3}$  is necessary for the RF transistor to sustain operation at voltages in excess of 100V.

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