1 Background

Integra devices with the IGNxxxx part number nomenclature are discrete high power devices which utilize GaN on SiC HEMT technology.

A GaN transistor is a depletion mode device, hence it requires a negative Gate voltage and a positive Drain supply voltage. The negative Gate voltage is required in order to pinch-off the Drain. An external Gate bias supply must be provided to apply the negative voltage to the Gate for setting I_{DQ}.

Integra E-K's (evaluation kits) typically include two transistors and one RF test fixture. One of the transistors is shipped in place in the RF test fixture and supplied with RF test data in order to allow high power RF correlation testing.

Drain supply charge storage is typically supplied by a 4700uF, 50V electrolytic capacitor.

2 Transistor Biasing and Turn-on Sequence

The following sequence should be followed when turning on the transistor.

1. The transistor is sensitive to ESD, and should be handled and tested in an ESD protected environment.
2. Make sure that the RF is turned off before installing the test fixture. Make sure that the proper pulse width and duty cycle has been properly set on the RF source prior to turning on the transistor. The transistor may be damaged if the RF source is not putting out the correct pulse format.
3. Hookup the test fixture to a test bench with a good 50 ohm load on both the input and the output side RF connectors. The output must have a high power load capable of handling ~3dB more than both the rated peak output power and the average output power. The test set Return Loss at the RF test fixture connectors (input and output) should be at least 26dB for testing purposes. For accurate correlation the test set Return Loss is recommend to be 30dB minimum.

4. Check the screw torque on the transistor clamp to ensure that the clamp has not loosened during shipment. The screws should be torqued sequentially to between 6-8 in/lbs.
5. The gate side bias supply voltage should be adjustable to apply from at least -2 to -5V to the fixture gate. This is done by hooking up the positive gate supply voltage to the fixture ground, and the negative supply to the blue bias lead as shown. Set the current limit on the Gate supply to 100mA. **Applying positive voltage to the Gate will damage the device.** The Gate supply must be able to source and sink current into the Gate. At low RF power, the negative supply applied to the Gate (BLUE) will sink current. At high input RF power, the Gate supply will need to source current. Most bench power supplies cannot source and sink current. This problem can be solved by putting a shunt resistor across the terminals of the Gate supply (See Rshunt in Figure 4). The resistor value should be Rshunt < V_{GS}, max/I_{GS},max. With V_{GS}, max = 4.5 V, I_{GS}, max = 10mA. Rshunt < 450 Ohms. Rshunt = 67 Ohms in Figure 4. The resistor power rating should be Pshunt > V_{GS}, max^2 / Rshunt. In Figure 3, Pshunt > (5*5)/82 Ohms = 0.3W. Hookup the Gate supply as shown in Figure 4, with the positive supply terminal +5V_{GG} on GND, and the negative supply terminal V_{GG} GND on the Gate Bias (BLUE) jack. Adjust the V_{GG} supply voltage to 5V. Verify that the voltage on the transistor Gate is -5V relative to the heat sink. Measure the resistance between V_{DD} (RED) and ground (BLACK). You should measure greater than 10K Ohms through the device Drain if the Gate supply voltage is properly applied. This value may change slightly depending on the drain leakage current, but you should measure a high impedance from drain to source since the channel is turned off.
6. Next connect the Drain supply V_{DD} as shown in Figure 3 with the supply turned OFF. Set the power supply current limit such that it, in conjunction with the charge storage capacitance, can handle the maximum peak current expected for the device. Make sure that the charge storage (4700uF) filter cap (Figure 2) is connected between the V_{DD} (RED) and V_{DD} GND (BLACK) terminals of the test fixture as shown in Figure 3. Next attach the power supply voltage sense leads to the V_{DD} and V_{DD} GND terminals, if available from the supply. Make sure that the power supply is in remote current sense mode. Otherwise, make sure to measure the Drain voltage at the terminals of the test fixture (RED to BLACK), and compensate for the voltage drop to the test fixture by adjusting the Drain supply voltage while testing the transistor. Hook up the main V_{DD} supply lines to the V_{DD} and V_{DD} GND terminals. Size the supply wires appropriately.
7. Turn on the +V_{DD} Drain power supply. There should be less than 10 mA of current drawn by the transistor Drain from the Drain supply, since the Gate bias is at -5V to keep the device in pinch off.

8. Adjust I_{DQ} (drain quiescent current) using the V_{GS} supply. Very slowly turn the V_{GS} supply voltage down in magnitude (10-50mV increments), to increase the Drain current to the desired I_{DQ}. A fine resolution power supply adjustment knob is highly desirable to prevent overdriving the gate voltage, inducing excessive I_D and potentially burning out the device. An Agilent E3610A power supply or equivalent is suitable. The Gate voltage should be around V_{GS} = -2.7V to get the rated I_{DQ} value.
9. Turn on the input RF power starting at low power (< 0.1W peak), and then increase until the desired output power is achieved. Correlation data is supplied with the clamped device. Please verify correlation before device removal per Section 6.
10. After testing is complete turn off the $+V_{DD}$ Drain supply voltage first. Leave the RF applied for about 5 seconds to discharge large charge storage Drain filter capacitor. Next, turn off the RF power. Lastly, turn off the Gate supply voltage.
11. The transistor should be handled in an ESD safe environment, with the operator properly grounded to prevent static discharge to the transistor, when removing and installing the transistor.
12. When inserting a new transistor, the device should be drain justified in the transistor slot. This means that the transistor should be pushed towards the drain side of the transistor slot before torqueing the clamp screws. The screws should be torqued sequentially to between 6-8 in/lbs. Before starting the turn on sequence of a new transistor please turn the Gate supply voltage back to 5V. Turn on the Gate supply, and measure the voltage on the Gate to GND. If you measure V_{GS} = -5V, proceed to step 7 above.
13. I_{DQ} SLOW TIME CONSTANT- If the RF is turned off from full power abruptly, the I_{DQ} will require several minutes to recover to the original bias setting. This is due to trapping effects. Please do not readjust the I_{DQ} as this will cause improper bias level adjustments. A better way to verify that the I_{DQ} is still correct would be to reduce the RF input power with a variable attenuator until the RF is off. The I_{DQ} in this case will be correct without waiting for time constant recovery.

3 Cooling

The transistor will dissipate power and requires adequate cooling. At a minimum a biscuit fan model BT2A1 or equivalent should be provided. The fan can provide 22CFM of airflow over the fins of the heat sink. A #4-40 threaded screw hole is located on the copper transistor carrier to monitor the flange temperature. The typical TF (flange temperature) for RF testing is 30°C±5°C.

4 Thermal Grease Application (if required)

Thermal grease was used for testing this part. Assuming that the transistor channel is clean, only a small dot of grease of 0.03-0.04" diameter is applied in the center of the slot. Do not use an excessive amount of grease. The grease pattern after transistor removal should not extend more than 0.25". The correct amount of grease is required to obtain a thin coat that will not degrade electrical contact. Use Wakefield 120 or equivalent thermal grease. Make sure that the clamp is properly seated on the top of the flange, and that the screws are torqued sequentially to between 6-8 in/lbs.

5 Temperature Compensation

The test fixture does not incorporate thermal compensation of the quiescent Drain current. The Gate bias voltage may need to be readjusted to maintain a constant I_{DQ}, if testing with large variations in operating temperature.

6 Device Correlation

The evaluation kit includes the test fixture, electrolytic cap, two transistors and RF test data. One of the devices is already clamped into the test fixture. The device has been tested at Integra as installed, and should be used for correlation purposes. Please compare data measured with Integra's RF data for the serial number installed in the test fixture. Please also consult with the datasheet for additional information.

7 Transistor Test Fixture Setup

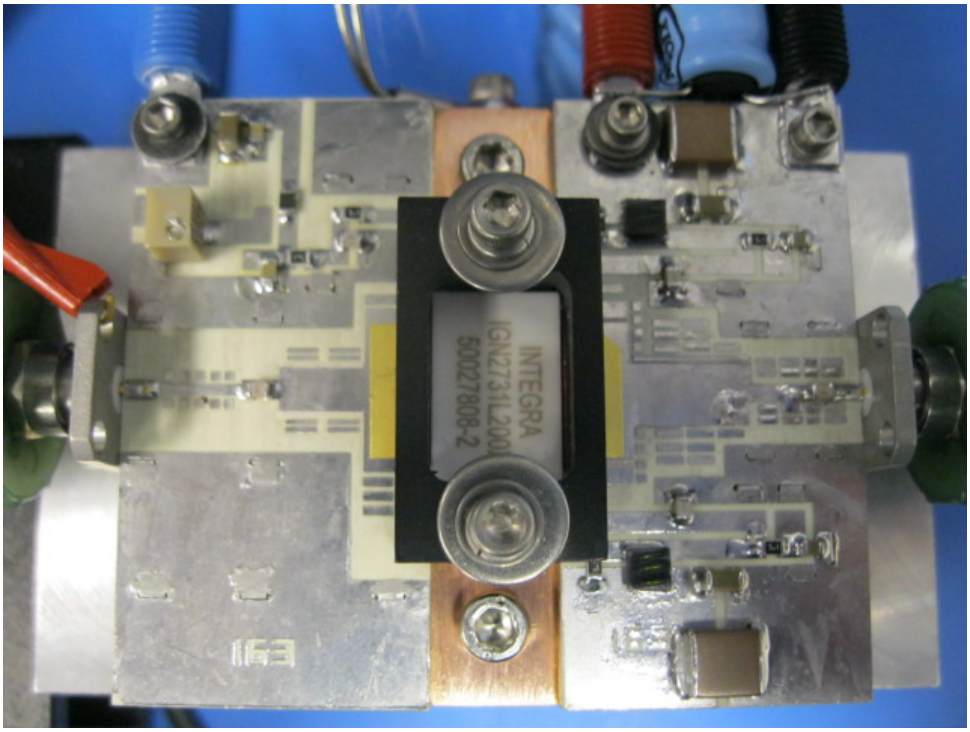

Figure 1- IGN2731L200 (typical) RF Test Fixture

Figure 2- Drain Supply Filter Cap Provided 4700uF (typical)

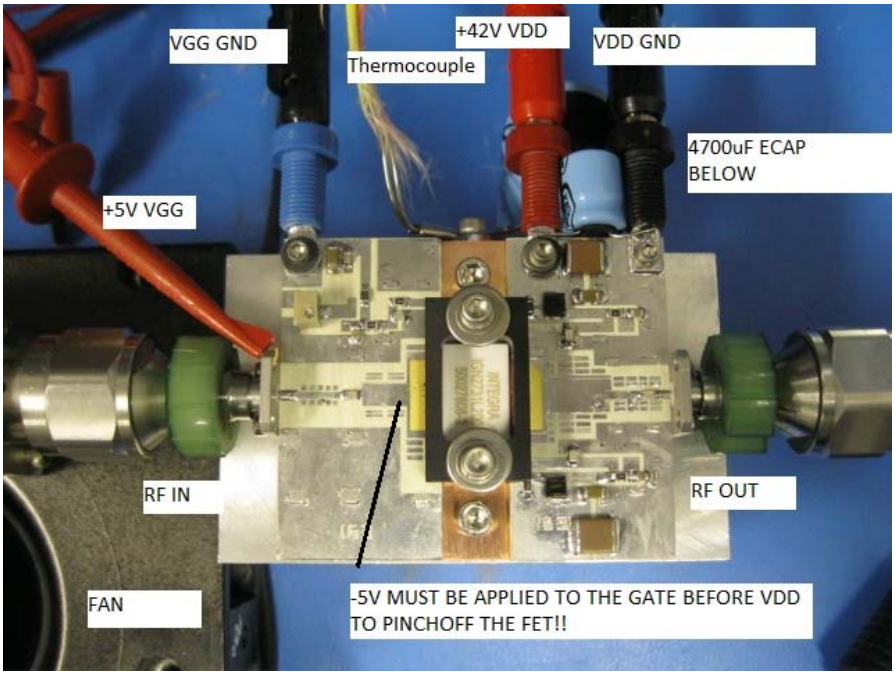

Figure 3- Test Fixture on RF Test Bench (typical)

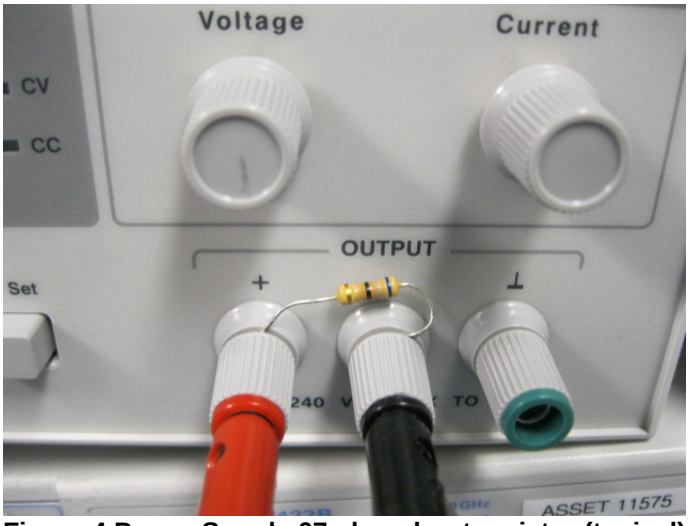

Figure 4 Power Supply 67 ohm shunt resistor (typical)