# High Efficiency Switch Mode GaN-based Power Amplifiers for P-Band Aerospace Applications

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*Abstract*— **Switch mode operation of a GaN HEMT device is explored to determine the performance and limitations of this technology for P-Band Pulsed waveforms. A combination of Class E and Inverse Class F amplifier operation is used to achieve high efficiency amplification. The measurements are based on a single 24mm GaN on SiC HEMT die operated at 50V bias, made by Integra Technologies, Inc. Harmonic tuning circuit techniques result in drain efficiency of 80%, and saturated power greater than 150W. The pulsed RF waveform used for this work has a pulse duration of 300uS and a 10% duty cycle. The operating frequencies at P-band are 420MHz to 450MHz. Measurements include bias modulation and drain sequencing circuit effects on amplifier efficiency. The presented results are part of an SBIR award from Jet Propulsion Laboratory / NASA, with the objective of designing and building a 1kW output power amplifier with greater than 80% efficiency for space exploration. To further facilitate the scaling of the presented techniques to a single ended part with 500W output power, we also present an investigation of a GaN on SiC transistor design to be operated at 100V bias at P-Band. The authors believe that the innovative approach discussed and proposed unleashes a new solution to the design of very high efficiency RADAR amplifiers for aerospace applications.**

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## 1. INTRODUCTION

Gallium Nitride (GaN) is a newly matured technology which has significant advantages in frequency band width, high junction temperature operation, high voltage breakdown and therefore high voltage operation [1] and radiation hardness [2] that can be applied to a variety of high reliability space applications. The GaN active epitaxial layers to form the HEMT device are typically grown on a silicon, silicon-carbide or sapphire substrate. For high power applications sapphire is not a good material choice due to its high thermal resistance. Due to its superior thermal conductivity, GaN on SiC is the ideal platform to harness all the benefits described above. GaN on silicon is a lower cost and lower performance alternative to GaN on SiC technology, which the authors believe is best suited for commercial applications in non-harsh environment. The goal of this investigation is to bench mark existing Integra Technologies, Inc. [3] GaN on SiC HEMT (High Electron Mobility Transistor) device technology for application to very high efficiency power amplifier design. The results of this work will be used to develop improved circuit and GaN HEMT designs to optimize high efficiency performance for future pulsed applications. The final goal will be to scale the device to a 500W or 1kW amplifier design that can be used for spacecraft RADAR (Radio Detection and Ranging) applications that require low power consumption.

### *Circuit Considerations*

The high efficiency amplification of RF signals can be achieved with Switch Mode Circuit techniques that employ specific load impedances for the fundamental and harmonics signals created by the transistor. The optimum impedance values and amplifier class of operation will be discussed as a reference for the investigation of GaN transistor performance. The derivation of an output impedance model for the GaN transistor is developed to allow for analysis of load impedance optimization. The fundamental and harmonic load impedances presented to the demonstration device by the test circuit are measured and compared to the optimum load impedances for Inverse Class F and Class E amplification. Resulting drain efficiency performance is presented with effects due to drain sequencing circuits, quiescent current levels, and gate bias modulation. RF device performance of the demonstration device is included for gain and saturated power.

### *GaN HEMT Structure and Design Goals*

This project uses the 24mm Integra Technologies GaN on SiC HEMT transistor type G154-200, designed for 50V operation. The die consists of 120 gate fingers each having 200um width for a total of 24mm gate periphery. It is based on a 0.5um GaN HEMT process, with gate and source field plates design, to achieve a typical breakdown voltage in excess of 125V. Under operating conditions, the die delivers >150W saturated power with over 80% drain efficiency, corresponding to a power density > 6W/mm. One approach to achieve 500W output power would require the combining of 4 such devices. For a 1kW power requirement, 2 such 500W devices would be combined on a pallet. The authors have previously demonstrated the challenges of designing

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high power transistors in GaN technology, with recent milestone achievement of a single ended 1kW transistor in S-band using a similar transistor [4]. The real challenge in the current project for P-band is to achieve high output power with efficiency exceeding 80%, which is addressed through class E and Inverse Class F circuit design techniques.

*High Voltage Design Considerations*

In order to meet the end objective of designing a power amplifier with 1kW output power and still retaining the very high efficiency of 80%, a different approach is also proposed, whereby modifying the GaN transistor design to increase the operating voltage from 50V to 100V. The redesign effort would translate into a higher power transistor with 2x higher power density and impedance, facilitating the power combining at the circuit level and allowing more tuning flexibility to meet the 80% minimum efficiency target. Therefore, the TCAD (Technology Computer Aided Design) simulator marketed by Silvaco Corp. has been used to simulate the electrical characteristics of the proposed GaN HEMT transistor with >250V breakdown voltage.

## 2. SWITCH MODE AMPLIFIER DESIGN

A switch mode amplifier consists of a device that acts like a switch, a parasitic device capacitance (Cds), and an output load (Zmatch) that presents specific impedances to the fundamental and harmonic frequencies. Figure 1 shows the ideal circuit diagram of a switch mode device.

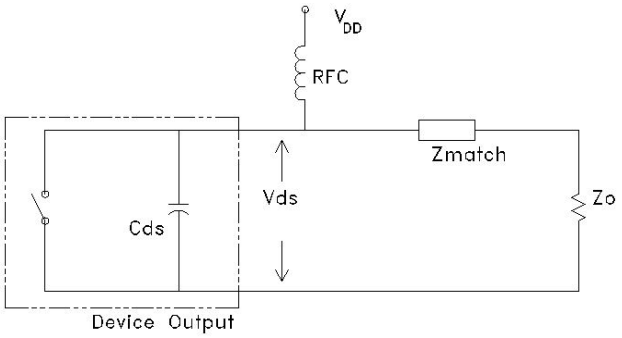


**Figure 1. Switch Mode Device**

Efficient switch mode amplification requires that the current waveform is at a minimum at the same time the voltage waveform is a maximum or vice versa across the drain of the device. To achieve this objective in a switch mode amplifier, the impedance match for the RF device must pass the fundamental and reflect the harmonics. At RF frequencies, the load impedance is greatly affected by the output shunt drain capacitance (Cds). Therefore any analysis of the output impedance requires the reference plane to be located at the current generator plane (CG) with a source impedance of effective drain source real resistance (Rds) as shown in Figure 2.

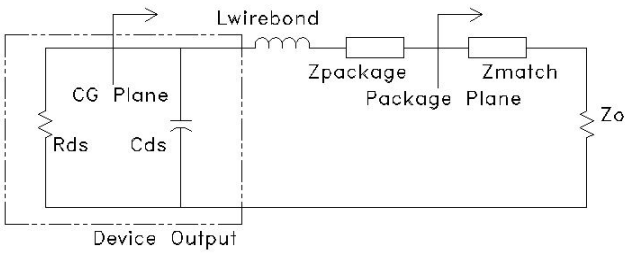


**Figure 2. Device Output Model**

For this work the investigation considers Inverse Class F and Class E switch mode operation. The ratio of the harmonic impedances to the fundamental load impedance determines the amplifier class of operation. Inverse Class F operation has high impedance for the even harmonics and low impedance for the odd harmonics. Class E operation requires that all harmonic load reactances are negative and similar in magnitude to the fundamental frequency load resistance. The optimum output load impedance for Class E and Inverse Class F operation are previously determined by Raab [5]. Normalized values are presented in Table 1.

**Table 1. Normalized Optimum Load Impedances**

| Harmonic | Inverse Class F | Class E |
|---|---|---|
| Fundamental | 1 | 1+j0.725 |
| Second | Open | -j1.785 |
| Third | Short | -j1.19 |

Although this description of switch mode amplifier operation is limited to the frequency domain analysis, the drain voltage (Vds) can reach 2.0 to 3.5 times the drain bias voltage ($V_{DD}$), depending on the class of switch mode operation. The peak value of Vds is determined by the effectiveness of Zmatch to reflect the harmonics and wave shape the voltage and current waveforms at the drain of the device [6]. For this work we estimate that the peak drain voltage is around 2.5 times Vds. Further investigation is planned with a nonlinear simulator to model the time domain waveform and estimate the peak drain voltage to determine a maximum safe operation value for $V_{DD}$.

## 3. DEVICE IMPEDANCE ESTIMATES

A test fixture was created with fundamental and harmonic matching elements to optimize the efficiency performance. The fixture design used an estimate of optimum device impedance for the fundamental frequency match and empirically tuned harmonic elements to optimize efficiency. The fundamental frequency matching elements use a low pass structure with series transmission lines and shunt capacitance. The harmonic frequency matching uses open and short circuit transmission line shunt elements to reflect the harmonics back into the device. The electrical lengths of the transmission line elements were adjusted to optimize the amplifier efficiency. A schematic representation of the output matching structure can be seen in Figure 7.

To determine the optimum fundamental device impedance, load pull data was measured at the device package reference plane and a model based on Figure 2 was created to approximate the measured values. The derivation of the model uses the combination of a calculation for Rds and an estimate of Cds by overlaying the model impedance to the load pull results. To approximate real impedance at the current generator, calculations for $R_{out(Inv\ F)}$ (Rds) can be determined by the equations below. These calculations are based on inverse Class F operation from Grebennikov [6].

$$R_{out(Inv\,F)} = \frac{\pi}{2} R_{out(B)} = \frac{\pi}{2} \frac{{V_{DD}}^2}{2\,(P_{RF})} \quad (1)$$

$$Rds = \frac{\pi\,(50V)^2}{4\,(160W)} = 12.3ohms \quad (2)$$

$R_{out(B)}$ is the real output impedance of a class B amplifier, $V_{DD}$ is the drain bias supply voltage, and $P_{RF}$ is the saturated output power of the device.

Starting with the calculated value for Rds, the value for Cds was adjusted to match the packaged device model (green marker in Figure 3) to the load pull result (red marker in Figure 3).

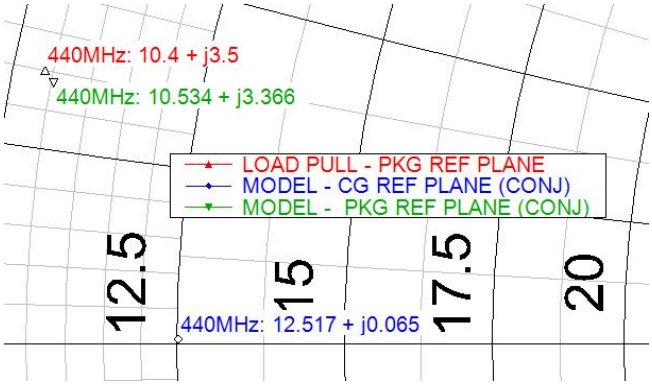


**Figure 3. Fundamental Impedance**

The resulting values for the device model are shown in Table 2.

**Table 2. Die Model Parameters – 24mm Device**

| Parameter | Load pull model |
|---|---|
| Cds (shunt output capacitance) | 12pf |
| Rds (current generator) | 12.5 ohms |

Load pull data was also measured at the harmonics and the CG impedances were de-embedded by modeling a shift in reference plane from the package plane to the CG plane, reference Figure 2. Normalized load impedance values at the CG reference plane for the fundamental and harmonics are shown in Table 3. The normalized fundamental impedance is 12.5ohms and the reference frequency is 440MHz for the demonstration device

**Table 3. Normalized Load Impedance – 24mm Device**

| Harmonic | 24mm Device |
|---|---|
| Fundamental | 1 |
| Second | 0.121-j1.41 |
| Third | 0.023-j0.391 |

The fundamental and harmonic impedances do not readily define the amplifier class of operation. The impedance results define an amplifier operation class that is a combination of Inverse Class F and Class E.

## 4. Device Performance

The measurement of the demonstration device in the test fixture shows exceptional performance with 80% efficiency at a power level of 160W. Figure 4 is the efficiency of the device at saturated power (Psat) over operating frequency range and the base plate temperature range of -25°C to +85°C. Psat is defined as 3dB gain compression from a reference power of 40W output.

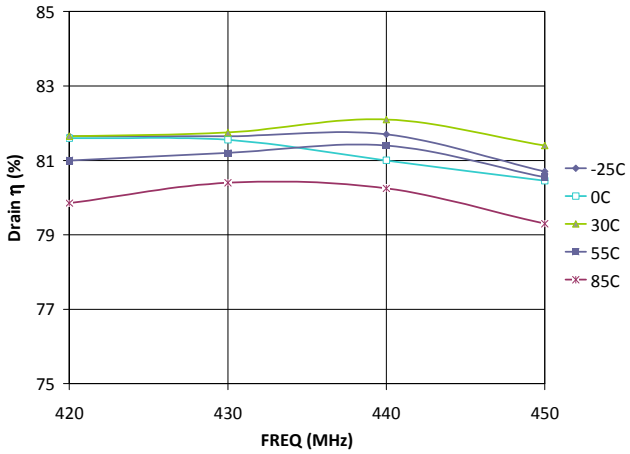


**Figure 4. Device Efficiency versus Temperature and Frequency at Saturated Power Output**

Figure 5 and Figure 6 show device saturated power and device gain over the operating frequency range and temperature.

To understand how additional amplifier circuits might affect the efficiency of the test device, measurements of efficiency with drain sequencing and gate modulation circuits are investigated. GaN HEMT devices are depletion mode FET devices that require protection from accidental saturated drain current (Idss). Negative gate source voltage (Vgs) is necessary to control the quiescent drain current of the device. A representative drain sequencing circuit using a low on resistance p-channel FET is shown in Figure 7. Power loss due to the quiescent drain source bias current during the pulse off time could be significant depending on the bias level. Modulation of Vgs to pinch off the device channel during the pulse off time can be accomplished with the circuit shown in Figure 8.

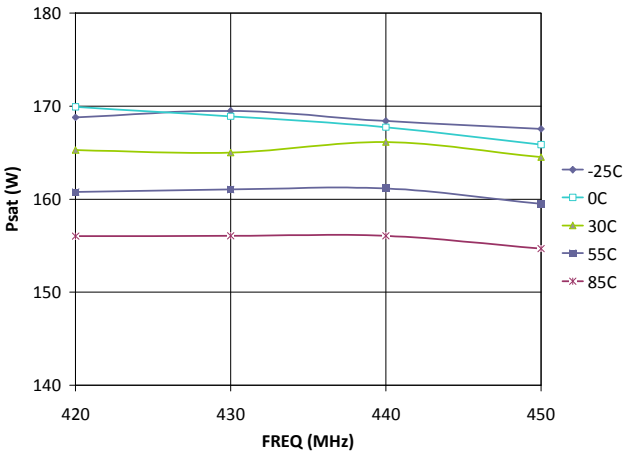


**Figure 5. Device Saturated Power (P3dB from 40W) versus Temperature and Frequency**

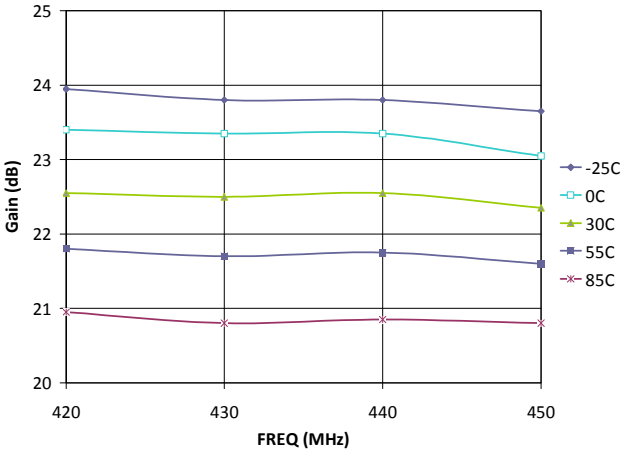


**Figure 6. Device Gain versus Temperature and Frequency at 160W output power**

Efficiency data from the demonstration device with the drain sequencing and gate modulation circuits added to the test fixture are shown in Figure 9. The efficiency is reduced approximately 1% with the addition of the drain sequencing circuit. Gate modulation does not significantly affect efficiency at saturated power and has some benefits if the device is operated at lower power levels.

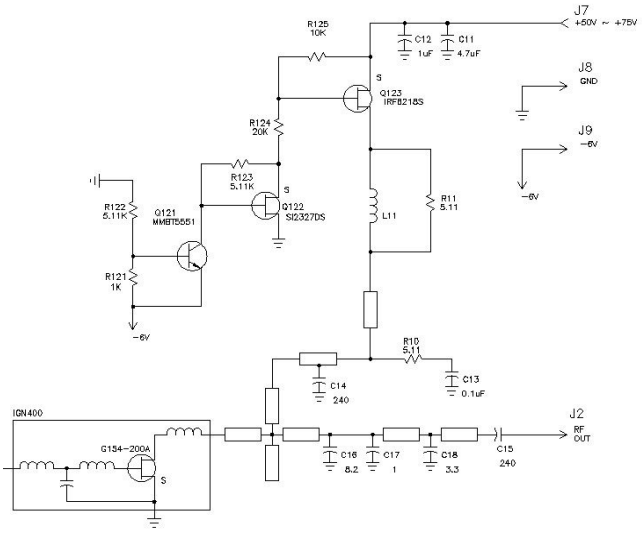


**Figure 7. Drain Sequencing Circuit**

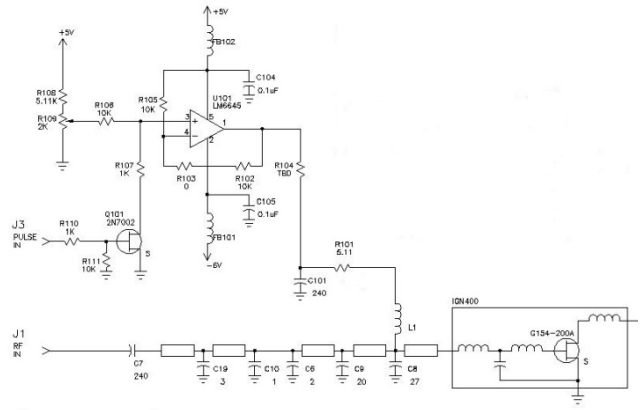


**Figure 8. Gate Modulation Circuit**

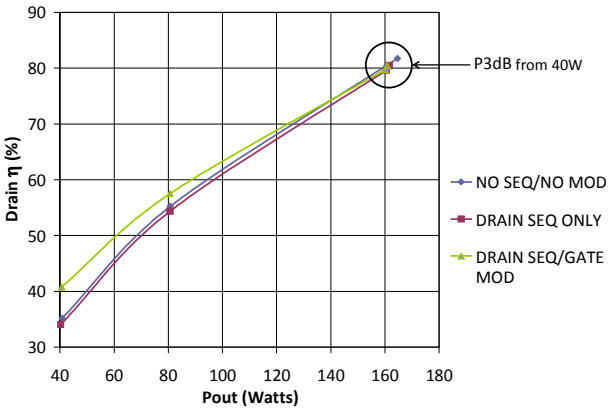


**Figure 9. Efficiency versus Output Power with drain sequence and gate modulation circuits, averaged values 420, 430, 440, 450MHz**

## 5. GaN HEMT Structure

In Figure 10 the cross section of the reference transistor used in this part of the project is shown as obtained from TCAD simulations. In particular, the voltage profile inside the device is shown when the drain is biased at 50V, under normal bias conditions. The voltage profile in the GaN buffer below the gate depends on the background Fe-concentration profile. Our TCAD model imports the measured Fe-profile as measured by SIMS analysis. The die is designed for a breakdown voltage ($BV_{dss}$) in excess of 125V.

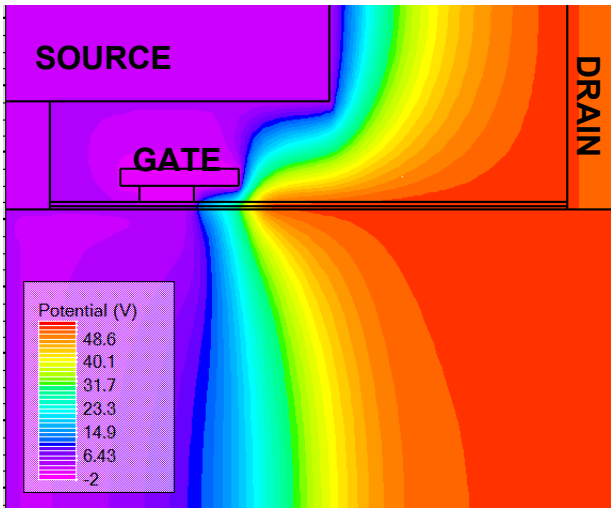


**Figure 10. TCAD cross section of reference GaN HEMT transistor used in this project. The drawing shows a 2D plot of the voltage profile with the drain bias at 50V.**

Figure 11 shows a set of Ids-Vds curves with gate-source bias set at different levels, showing the onset of breakdown at voltage exceeding 125V. The data are generated for a transistor cell having 1mm total gate periphery, so the current level can be interpreted as the amperes per millimeter current density figure of merit. The gate-source bias is varied in 1V steps, starting from +1V down to 0V, -1V and -2V, -3V and -4V and the current difference between two adjacent curves is an indication of the intrinsic trans-conductance (gm) the device is able to achieve. For the Ids-Vds curve at Vgs = 0V, the estimated intrinsic trans-conductance is 0.25 S/mm. Due to source and drain resistance, coupled with ohmic contact resistance at the source and drain electrodes, the measured extrinsic trans-conductance is closer to 0.2 S/mm. The die has a measured input capacitance (Ciss) of ~2.5pF/mm, which is due to the gate to channel depletion capacitance, gate field plate to drain dielectric capacitance, and gate metal to source field plate dielectric capacitance. From the measured data we can extract the cutoff frequency of this technology to be >10GHz. (Ft = gm / 2 π Ciss = 0.2S / 6.28 x 2.5e-12pF = 12.7 GHz). High cutoff frequency Ft is a requirement for being able to implement harmonic tuning techniques and achieve high efficiency power amplification. The maximum current ($I_{MAX}$) at Vgs = +1V is around ~0.8A/mm. At 50V bias ($V_{DD}$), with a ~10V saturated voltage ($V_{SAT}$), the maximum power density ($PD_{MAX}$) is:

$$PD_{MAX} = \frac{(V_{DD}-V_{SAT})I_{MAX}}{4} \quad (3)$$

$$PD_{MAX,50V} = \frac{(50V-10V)0.8A/mm}{4} = 8W/mm \quad (4)$$

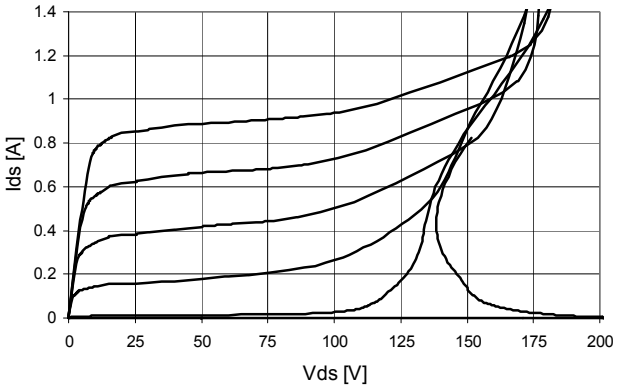


**Figure 11. TCAD generated Ids-Vds curves showing BVDSS in excess of 125V. The data are for a transistor cell of 1mm in gate periphery. I-V curves are for VGS = +1V (top), 0V, -1V -2V, -3V and -4V (bottom).**

To understand thermal stress on the 24mm transistor die at this power density, channel temperature can be considered. Several techniques to compute the die thermal resistance have been summarized by H. F. Cooke in Chapter 5 of reference [7]. The thermal resistance ($\theta_{jc}$) for the 24mm die is calculated to be ~1.0°C/W, which accounts for the bare GaN on SiC die, AuSn solder, and package flange. The approximate peak channel temperature ($T_{channel}$) can be calculated by:

$$T_{channel} = T_{Baseplate} + \theta_{jc}(P_{DC} - P_{RF}) \quad (5)$$

$$P_{DC} = \frac{P_{RF}}{\eta} \quad (6)$$

$P_{DC}$ is the input DC power to the device, $P_{RF}$ is the RF power presented to the load, and η is the drain efficiency of the amplifier. With 160W RF output power and 80% drain efficiency the DC power is 200W. Therefore the dissipated power $P_{DC} - P_{RF}$ is 40W. For a base plate temperature of 85°C, the calculated peak junction temperature is 125°C.

## 6. High Voltage Design Considerations

Next, we have used the same TCAD simulation project and modified the transistor design to obtain a breakdown voltage in excess of 250V. Typically, that is achieved by extending the gate-drain distance, or drift region of the transistor, but also adjusting the location of the field plates. In order not to increase the input capacitance Ciss significantly, it is

important to keep the gate electrode structure unchanged as much as possible; hence most of the field plates re-design is focused around the source connected field plate. Further improvements to the transistor design address the epi design, which translate into a slightly increased epi resistivity. A process split implemented when ordering the modified epi and when manufacturing the new device may result in further improvements to the data predicted with the TCAD simulator. In Figure 12 the cross section of the proposed transistor for a future phase of the project is shown as obtained from TCAD simulations. The die is designed for a breakdown voltage in excess of 250V. In particular, the voltage profile inside the device is shown when the drain is biased at 100V, under normal bias conditions.

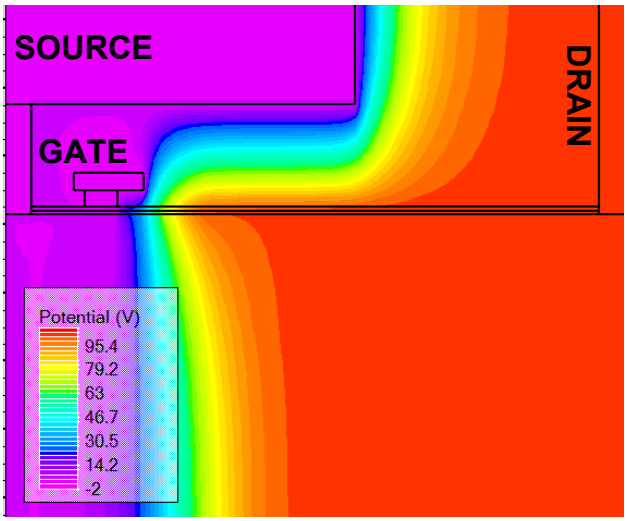


**Figure 12. TCAD cross section of high voltage proposed GaN transistor design for next phase in this project. The drawing shows a 2D plot of the voltage profile with the drain bias at 100V.**

Figure 13 shows a set of Ids-Vds curves with gate-source bias set at different levels, (+1V, 0V, -1V, -2V, -3V and -4V) showing the onset of breakdown at a drain voltage exceeding 250V. The data are generated for a transistor cell having 1mm total gate periphery, so the current level can be interpreted as the amperes per millimeter current density figure of merit. The gate-source bias is varied in 1V steps, so the current difference between two adjacent curves is an indication of the intrinsic trans-conductance gm the device is able to achieve. From the simulated Ids-Vds curve at Vgs = 0V, the estimated intrinsic trans-conductance is still close to 0.25 S/mm, only slightly reduced compared to the reference design. Again, due to source and drain resistance, coupled with ohmic contact resistance at the source and drain electrodes, we anticipate the measured extrinsic trans-conductance to be ~0.2 S/mm; the extra resistance due to the longer drift region is already included in the simulations data so we anticipate the parasitic resistances to stay the same. Since the gate structure has not been altered in the modified design, but only the source field plate has been extended, we expect the die to have an input capacitance Ciss of ~2.75pF/mm, or ~10% higher than in the 50V design. We can then extrapolate the cutoff frequency of this newer technology to be still >10GHz. High cutoff frequency Ft is a very important requirement for being able to implement harmonic tuning techniques needed for power amplification with efficiency >80%, and care must be taken to make sure that achieving higher bias operation of 100V does not come at the expense of lower Ft. As shown in figure 13, the maximum current $I_{MAX}$ at Vgs = +1V is estimated ~0.8A/mm. At 100V bias $V_{DD}$, with a ~20V saturated voltage $V_{SAT}$ due to the longer drift region, the predicted maximum power density is estimated to be:

$$PD_{MAX,100V} = \frac{(100V-20V)0.8A/mm}{4} = 16W/mm \qquad (7)$$

This result is ~2x what has been achieved in the present report using the reference device.

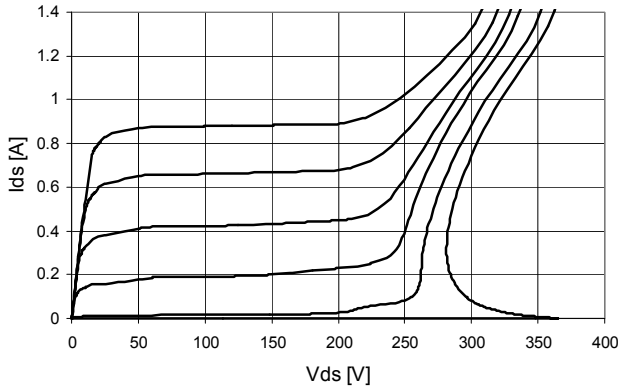


**Figure 13. TCAD generated Ids-Vds curves showing BVDSS in excess of 250V. The data are for a transistor cell of 1mm in gate periphery. I-V curves are for VGS = +1V (top), 0V, -1V, -2V, -3V and -4V (bottom).**

Therefore, in order to get 150W saturated output power when using 100V GaN devices, the total gate periphery required is ½ of the 24mm used with the 50V GaN demonstration device, i.e., 12mm. The channel temperature calculation for a similar 12mm transistor die operating at 100V and delivering the same RF output power as the demonstration device would still result in a value of 125°C at a base plate temperature of 85°C. Care must be taken in the layout of the new 100V biased transistor to ensure that the thermal resistance will not be too high, as the TCAD simulations do predict a 2x power density. Therefore to keep same junction temperature as the reference device tested in the present phase of the project, the active area of the die will have to be kept the same as for the 50V device, even though the total gate periphery now is only 12mm. Several layout designs will be explored that reduce the number of gate fingers from 120 to 100, 80 and 60 without reducing the die physical width or even the active die area, which calls for an increase in design pitch (gate to gate spacing) while also decreasing the gate finger length. The best die design will be selected for the final 1kW amplifier.

A comparison of the key parameters for the existing 50V and the proposed 100V GaN on SiC HEMT device is summarized in Table 4.

**Table 4. Comparison of key parameters for the 50V and 100V GaN on SiC HEMT Device**

| Parameter | 50V Design | 100V Design |
|---|---|---|
| $BV_{dss}$ [V] | 125 | 250 |
| $V_{DD}$ [V] | 50 | 100 |
| $V_{SAT}$ [V] | 10 | 20 |
| $I_{MAX}$ [A/mm] | 0.8 | 0.8 |
| $PD_{MAX}$ [W/mm] | 8 | 16 |
| Ciss [pF/mm] | 2.5 | 2.75 |
| gm [S/mm] | 0.2 | 0.2 |
| Ft [GHz] | 12.7 | 11.6 |

## 7. SUMMARY

It has been shown that very high efficiency power amplification at P-band is achievable with existing GaN on SiC HEMT device technology from Integra Technologies, Inc. The ultimate goal of this research is to enable very high power and highly efficient amplifiers for P-Band, in excess of 500W and greater than 80% efficiency. Scaling existing 50V technology to achieve greater than 500W will create lower device impedances that will be more difficult to match for high efficiency operation. Increasing the drain voltage from 50V to 100V is an attractive option. The power density (Watt/mm) increases by a factor of 2. For the same RF output power the Cds decreases by a factor of 2 and the Rds increases by a factor of 4. The reduction in Cds will enable a larger range of harmonic tuning solutions for best efficiency. TCAD simulations have shown that such a new GaN device, operating at 100V bias, is indeed achievable.

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## BIOGRAPHY

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***Dr. Gabriele F. Formicone*** *received his Ph. D. in Electrical Engineering from Arizona State University. He has over 15 years of hands-on industry experience in the design of RF/Microwave power transistors for commercial linear applications in the wireless infrastructure market and for military / defense pulse applications in radar and avionics systems. His industrial expertise covers Silicon Bipolar, Vertical and Lateral DMOS transistors, and GaN HEMT RF power technologies, spanning from TCAD simulations for transistor design and process optimization, to transistor layout, and project management with wafer fab and foundry operations management.*