

## L-Band TACAN Transistor

The high power pulsed transistor device part number IB1012S500 is designed for systems operating over the instantaneous bandwidth of 1025-1150 MHz. While operating in class C mode under DME pulsing conditions and  $V_{cc}=50V$ , this common base device supplies a minimum of 500 watts of peak pulse power. It utilizes a low loss internal input impedance matching structure to yield maximum device gain and to ease the implementation of external matching circuitry. The new generation bipolar transistor geometry utilizes a gold metallization system to achieve maximum reliability. Emitter ballast resistance is incorporated on the active cell for optimum thermal distribution and maximum reliability. All devices are 100% screened for large signal RF parameters.



### Silicon Bipolar

- Ultra-high  $f_T$

### Class C Operation

- High Efficiency

### Common Base Configuration

- Single Power Supply

### Gold Metal

- Maximum Reliability

### Emitter Ballasting

- Optimum Thermal Distribution

### Internal Impedance Matching

- Ease of Use
- Ultra-low Loss Design

### Be0 Package

- Unmatched Thermal Reliability

### RF Test Fixture

- Broadband
- Matched to 50Ω
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning Allowed
- Micro-strip structure on soft pc board with dielectric constant 10.2

## TYPICAL DATA

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General Information	Test Sequence	Freq	PIN	RL	POUT	GP	dG	IC	nc	Droop	VSWR-S	VSWR-LMT	
IB1012S500	Name	(MHz)	(W)	(dB)	(W)	(dB)	(dB)	(A)	(%)	(dB)	1.5:1	3:1	
Date:	3/26/2009												
Assbly Lot - SN :	D4126-2	Nominal	1025	50	-16.0	543	10.36	20.000	54.3	0.05	S	P	
Wafer :	BV3B-1-7												
Test Fixture :	2455-2500	Nominal	1090	50	-13.0	538	10.32	0.09	18.200	59.1	0.09	S	P
Pass / Fail :	Device Passes												
OPERATOR:	FB	Nominal	1150	50	-16.0	532	10.27	17.500	60.8	0.03	S	P	
Vcc=50V	Pulse: 10us-1%												

**MAXIMUM RATINGS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Collector-Emitter Voltage	$V_{CES}$	--	75	V	--
BD	Emitter-Base Voltage	$V_{EBO}$	--	2	V	--
BD	Storage Temperature Range	$T_{STG}$	-55	+150	°C	--
BD	Operating Junction Temperature Range	$T_J$	-55	+200	°C	--
Note	Screen 'BD' = parameter qualified By Design.					

**THERMAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	TBD	°C/W	$V_{CC}=50V$ , Pulse format=DME 10 $\mu$ s, 1%, $T_F=25\pm 5^\circ C$ , $P_{IN}=50W$ , $N_C=50\%$
Note	Screen 'BD' = parameter qualified By Design.					

**PROCESSING SPECIFICATIONS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

**DC ELECTRICAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Collector-Emitter Breakdown Voltage	$BV_{CES}$	75	--	V	$I_C = 40mA$ , $V_{BE} = 0V$ , $T_F = 25\pm 5^\circ C$ .
100%	Zero Base Voltage Collector Leakage Current	$I_{CES}$	--	1.0	mA	$V_{CE} = 50V$ , $V_{BE} = 0V$ , $T_F = 25\pm 5^\circ C$ .
100%	DC Current Gain	$H_{FE}$	20	100	--	$V_{CE} = 5V$ , $I_C = 500mA$ , $T_F = 25\pm 5^\circ C$ .

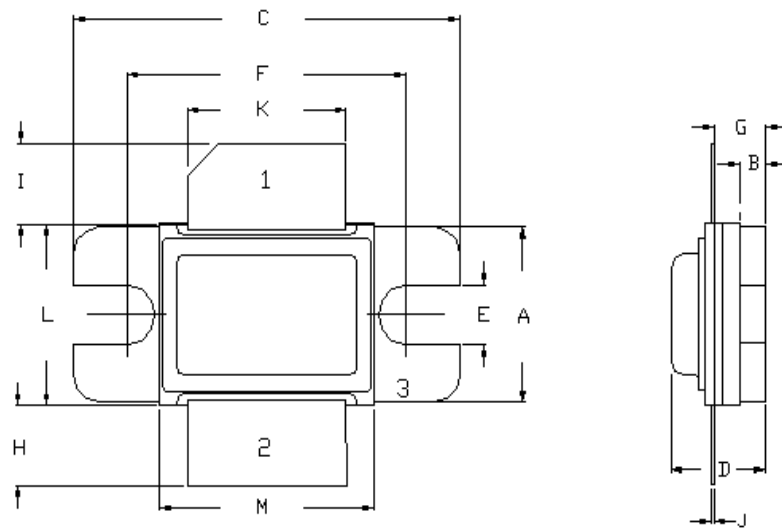
**RF ELECTRICAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	RL	-18	-10	dB	$V_{CC}=50V$ , $P_{IN}=50W$ , Pulse = Note 2, $T_F=25\pm5^\circ C$ , $F=F1$ .
BD	Maximum Overdrive	$P_{IN(MAX)}$	--	67	W	$V_{CC}=50V$ , Pulse = Note 2, $T_F=25\pm5^\circ C$ , $F=F1$ .
100%	Power Gain	$G_P$	10.00	11.50	dB	$V_{CC}=50V$ , $P_{IN}=50W$ , Pulse = Note 2, $T_F=25\pm5^\circ C$ , $F=F1$
100%	Output Power	$P_{out}$	500	706	W	$V_{CC}=50V$ , $P_{IN}=50W$ , Pulse = Note 2, $T_F=25\pm5^\circ C$ , $F=F1$
100%	Collector Efficiency ( $P_o/I_c/V_{CC}$ )	$N_C$	50	75	%	$V_{CC}=50V$ , $P_{IN}=50W$ , Pulse = Note 2, $T_F=25\pm5^\circ C$ , $F=F1$ .
100%	Pulse Amplitude Droop	Droop	-0.5	0.5	dB	$V_{CC}=50V$ , $P_{IN}=50W$ , Pulse = Note 2, $T_F=25\pm5^\circ C$ , $F=F1$ .
100%	Gain Flatness	$\Delta G$		1.5	dB	Delta between highest gain and lowest gain from 960-1215MHz
100%	Stability into 1.5:1 VSWR	VSWR-S	--	--	--	$V_{CC}=50V$ , $P_{IN}=50W$ , Pulse = Note 2, $T_F=25\pm5^\circ C$ , $F=F1$ . Rotate 1.5:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse.
100%	Load Mismatch Tolerance	VSWR-LMT	3:1	--	--	$V_{CC}=50V$ , $P_{IN}=50W$ , Pulse = Note 2, $T_F=25\pm5^\circ C$ , $F=F1$ . Rotate 3:1 output VSWR through 360° phase. Survival.
Note 1	F1 = 1025/1090/1150 MHz.					
Note 2	Pulse width = DME (10us, 1%)					
Note 3	$T_F$ = Device flange temperature.					
Note 4	Screen 'BD' = parameter qualified By Design.					

**RF TEST FIXTURE IMPEDANCE CHARACTERISTICS**

Frequency (MHz)	$Z_{IF}$ ( $\Omega$ )	$Z_{OF}$ ( $\Omega$ )
1025	1.44-j1.38	1.58-j2.08
1090	1.47-j1.07	1.60-j1.73
1150	1.59-j0.85	1.68-j1.47
Impedance Definition		

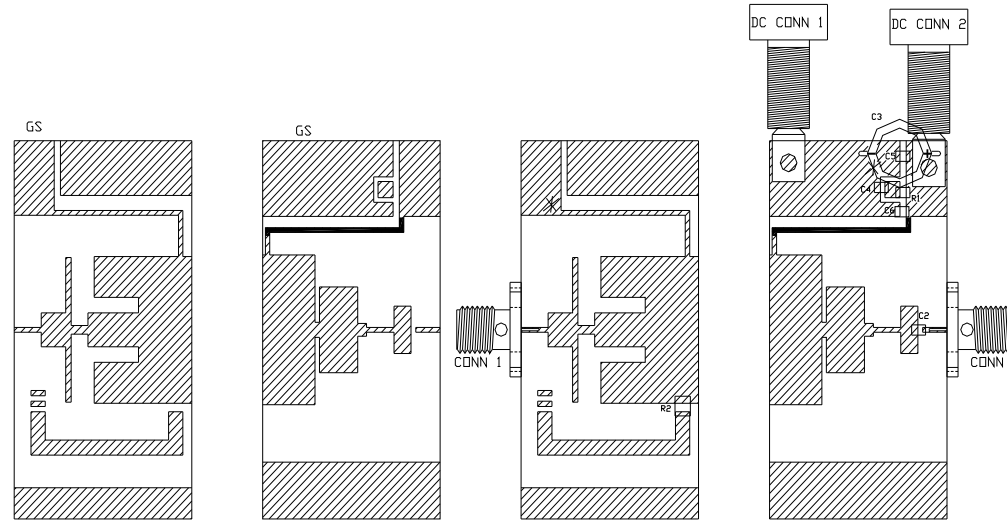
**PACKAGE DIMENSIONAL OUTLINE DRAWING**



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.380	0.390	9.65	9.91
B	0.055	0.065	1.39	1.65
C	0.895	0.905	22.73	22.99
D	0.225	0.235	5.71	5.97
E	0.125	0.135	3.18	3.43
F	0.645	0.655	16.38	16.64
G	0.120	0.130	3.12	3.25
H	0.160	0.190	4.06	4.82
I	0.160	0.190	4.06	4.82
J	0.004	0.006	0.10	0.15
K	.0365	0.375	9.27	9.52
L	0.395	0.405	10.03	10.29
M	0.495	0.505	12.57	12.82

PIN SCHEDULE	
1	COLLECTOR
2	EMITTER
3	BASE

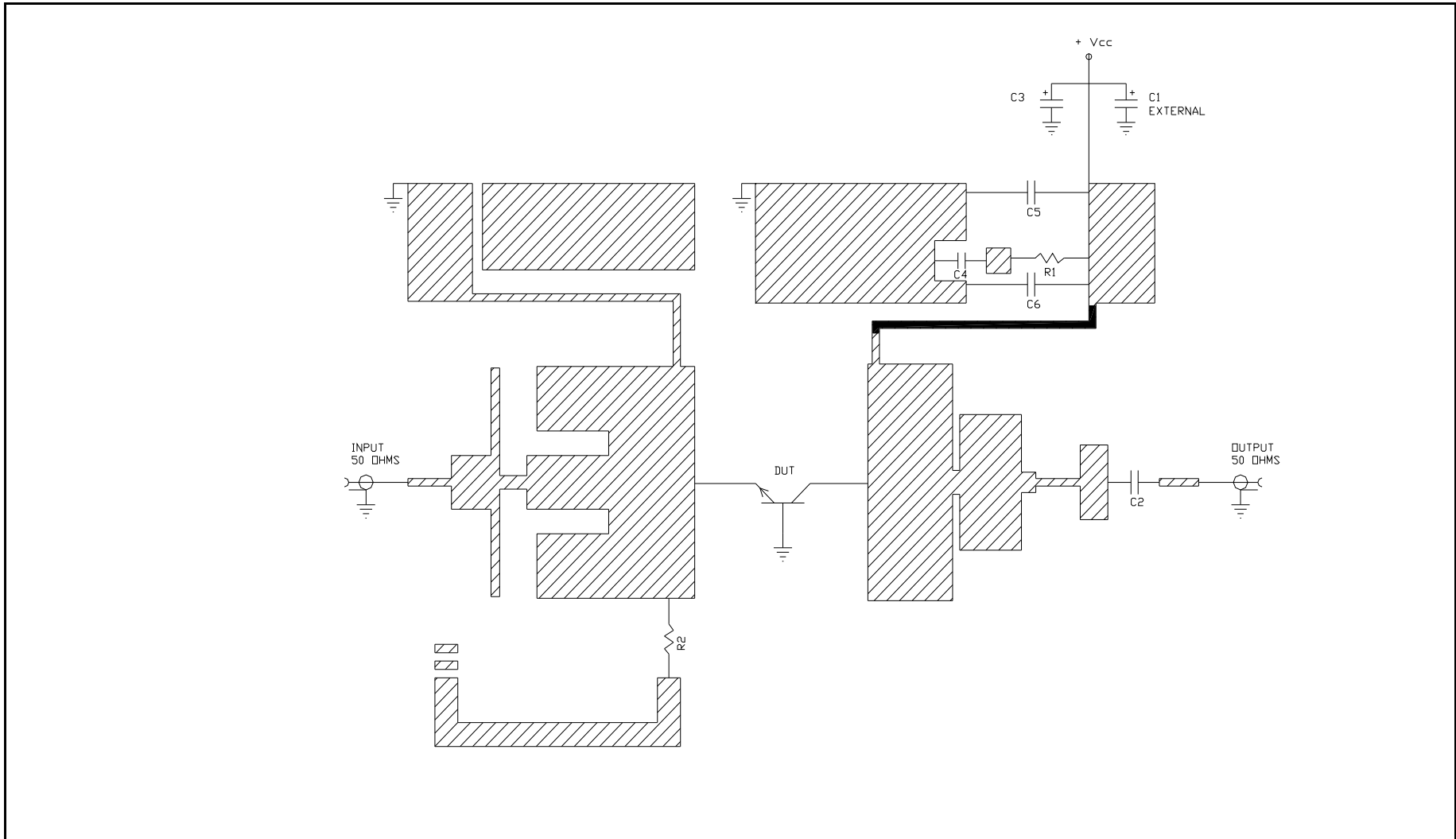
**RF TEST FIXTURE**



COMPONENT	DESCRIPTION
DUT	TRANSISTOR #IB1012S500 MOUNT HARD TO THE RIGHT
PC BOARD	ROGERS #RD 6010.2 .026" 1oz Cu
C1 (NOT SHOWN)	STORAGE ELECTROLYTIC CAPACITOR 4700uF / 50V
C2	CHIP CAPACITOR ATC100A - 100pF
C3	ELECTROLYTIC CAPACITOR 68uF / 63V
C4	CHIP CAPACITOR 0.1uF
C5	CHIP CAPACITOR 2uF
C6	CHIP CAPACITOR ATC 39pF
R1	CHIP RESISTOR 6.8ohms
R2	CHIP RESISTOR 50ohms
GS (2 PLACES)	GROUND SHIM, COPPER, TH=0.001"
CONN 1, CONN 2	SMA CONNECTOR, QS #2052-5636-02
INPUT PC BOARD CARRIER	2 INCH BRASS-03 (1")
OUTPUT PC BOARD CARRIER	2 INCH BRASS-03 (1")
TRANSISTOR CARRIER	2 INCH COPPER-02 (P54)
TRANSISTOR CLAMP	NORYL CLAMP-03 (P54)
ALUMINUM HEAT SINK	2 INCH HEATSINK-11
DC CONN 1	BANANA JACK, BLACK
DC CONN 2	BANANA JACK, RED
NOTE	FIXTURE HARDWARE DRAWINGS AVAILABLE ON REQUEST



**RF TEST FIXTURE ELECTRICAL SCHEMATIC**



**DEFINITIONS**

<b>Data Sheet Status</b>	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
<b>Maximum Ratings</b>	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only and operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

**WARNING**

<b>Product and environmental safety - toxic materials</b>
This product contains beryllium oxide. The product is entirely safe provided that the BeO base is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with general or domestic waste.

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