

S-Band Radar Transistor

The high power pulsed radar transistor device part number IB3135M100 is designed for S-Band radar systems operating over the instantaneous bandwidth of 3.1-3.5 GHz. While operating in class C mode this common base device supplies a minimum of 100 watts of peak pulse power under the conditions of 100µs pulse width and 10% duty cycle over the frequency range of 3.1-3.5 GHz. All devices are 100% screened for large signal RF parameters, including power gain compression. Excellent spectral stability into output mismatch over a broad input power range make it ideal for use in reliable high power solid state transmitters. The test fixture includes a passive amplitude sloping network to insure that the device is not overdriven as the operating frequency decreases.



Silicon Bipolar
 – Ultra-high f_T

Class C Operation
 – High Efficiency

Common Base Configuration
 – Single Power Supply

Gold Metal
 – Maximum Reliability

Emitter Ballasting
 – Optimum Thermal Distribution

Internal Impedance Matching
 – Ease of Use
 – Ultra-low Loss Design

BeO Package
 – Unmatched Thermal Reliability

RF Test Fixture
 – Broadband
 – Matched to 50Ω
 – Long-term Correlation
 – 100% Device RF Screening
 – No External Tuning Allowed

Insertion Phase Marking
 – 5° Increment Marking

Patents Issued
 – US 6181200 B1
 – US 6331931 B1

TYPICAL DATA TYPICAL DATA TYPICAL DATA TYPICAL DATA

General Information	Freq (GHz)	PW (us)	Duty (%)	Vcc (V)	P _{IN} (W)	IRL (dB)	P _{OUT} (W)	G _P (dB)	I _C (A)	n _c (%)	Droop (dB)	VSWR 1.5:1	VSWR 2:1
Assbly Lot - SN : D2298-2	3.100	100	10	36.0	16.3	-13	147	9.5	9.23	44	-0.40	S	P
	3.200	100	10	36.0	16.3	-14	151	9.7	9.48	44	-0.40	S	P
	3.300	100	10	36.0	16.3	-13	144	9.5	8.83	45	-0.25	S	P
	3.400	100	10	36.0	16.3	-13	131	9.1	8.45	43	-0.20	S	P
	3.500	100	10	36.0	16.3	-17	120	8.7	7.75	43	-0.20	S	P

MAXIMUM RATINGS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Collector-Emitter Voltage	V_{CES}	--	70	V	$V_{BE}=0V$.
BD	Storage Temperature Range	T_{STG}	-65	+200	°C	--
BD	Operating Junction Temperature Range	T_J	-55	+200	°C	--
Note	Screen 'BD' = parameter qualified By Design.					

THERMAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	0.34	°C/W	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{OUT}=100W, N_C=38\%$.
Note	GB = Guard Band. Screen 'BD' = parameter qualified By Design.					

PROCESSING SPECIFICATIONS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification.
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071.6, Test Condition C.
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

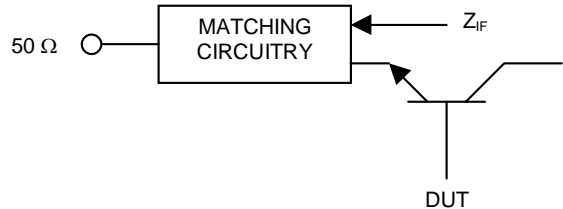
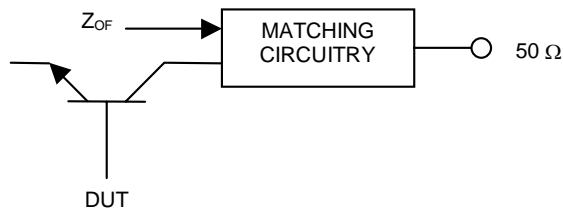
DC ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Collector-Emitter Breakdown Voltage	BV_{CES}	70	--	V	$I_C=30mA, V_{BE}=0V, T_F=25\pm5^\circ C$.
100%	Zero Base Voltage Collector Leakage Current	I_{CES}	--	6.0	mA	$V_{CE}=30V, V_{BE}=0V, T_F=25\pm5^\circ C$.
100%	DC Current Gain	H_{FE}	10	120	--	$V_{CE}=5V, I_C=0.1A, T_F=25\pm5^\circ C$.

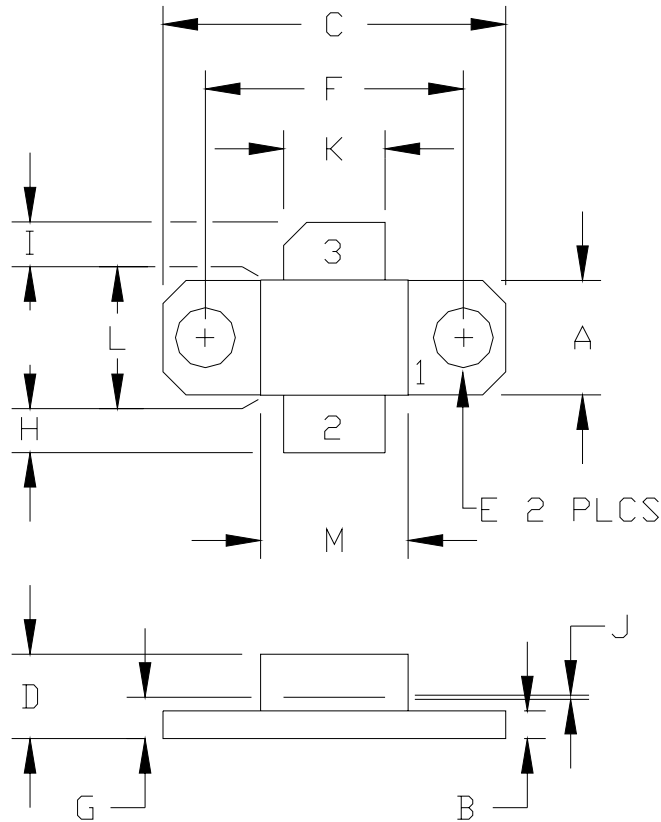
RF ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	IRL1	8	--	dB	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, F=F1.$
100%	Input Return Loss	IRL2	9	--	dB	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN2}, F=F2.$
100%	Input Return Loss	IRL3	10	--	dB	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN3}, F=F3.$
100%	Output Power	P_{O1}	100	--	W	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, F=F1.$
100%	Output Power	P_{O2}	100	--	W	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN2}, F=F2.$
100%	Output Power	P_{O3}	100	--	W	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN3}, F=F3.$
100%	Collector Efficiency ($P_O/I_C/V_{CC}$)	NC_1	38	--	%	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, F=F1.$
100%	Collector Efficiency ($P_O/I_C/V_{CC}$)	NC_2	38	--	%	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN2}, F=F2.$
100%	Collector Efficiency ($P_O/I_C/V_{CC}$)	NC_3	38	--	%	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN3}, F=F3.$
100%	Pulse Amplitude Droop	D1	--	0.7	dB	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, F=F1.$
100%	Pulse Amplitude Droop	D2	--	0.7	dB	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN2}, F=F2.$
100%	Pulse Amplitude Droop	D3	--	0.7	dB	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN3}, F=F3.$
100%	Output Power Compression = $10 \cdot \text{LOG}(P_{OC}/P_O)$	OPC1	+0.02	+0.48	dB	P_{OC} measured with P_{IN} increased by 0.5dB at $F=F1.$
100%	Output Power Compression = $10 \cdot \text{LOG}(P_{OC}/P_O)$	OPC2	+0.02	+0.48	dB	P_{OC} measured with P_{IN} increased by 0.5dB at $F=F2.$
100%	Output Power Compression = $10 \cdot \text{LOG}(P_{OC}/P_O)$	OPC3	+0.02	+0.48	dB	P_{OC} measured with P_{IN} increased by 0.5dB at $F=F3.$
100%	Output Power Flatness = $10 \cdot \text{LOG}(P_{OMAX}/P_{OMIN})$	OPF	--	1.5	dB	Calculate from P_O at each frequency $F.$
100%	Delta Insertion Phase Variation	d-IP	-30	+30	Deg	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN3}, F=F3, \text{Mark in } 5^\circ \text{ increments.}$
100%	Stability into 1.5:1 VSWR with +0.75dB overdrive	VSWR-S	--	--	--	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, P_{IN2}, P_{IN3}, F=F1, F2, F3. \text{ Repeat } P_O \text{ with } P_{IN} \text{ increased by } 0.75\text{dB. Rotate } 1.5:1 \text{ output VSWR through } 360^\circ \text{ phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse. All non-harmonically related signals must be at least } -65 \text{ dBc.}$
100%	2:1 Load Mismatch Tolerance	LMT	--	--	--	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, P_{IN2}, P_{IN3}, F=F1, F2, F3. \text{ Rotate } 2:1 \text{ output VSWR through } 360^\circ \text{ phase. Post test } P_O = \text{Pre test } P_O \pm 5W.$
Note	$V1 = 36V; PW1 = 100\mu s; DF1 = 10\%; P_{IN1} = P_{IN2} = P_{IN3} = 16.3 \text{ W}; F1 = 3.10 \text{ GHz}, F2 = 3.30 \text{ GHz}, F3 = 3.50 \text{ GHz.}$					
Note	$T_F = \text{Device flange temperature. Screen 'BD' = parameter qualified By Design.}$					
Note	Parts are binned and marked in 5 degree increments for Insertion Phase IP : ITI-1, -2, -3, -4, -5, -6, -7, -8, -9, -10, -11, -12.					

BROADBAND RF TEST FIXTURE IMPEDANCE CHARACTERISTICS

Frequency (GHz)	Z_{IF} (Ω)	Z_{OF} (Ω)
3.10	$3.5 - j5.7$	$2.6 - j7.2$
3.20	$3.2 - j5.5$	$2.2 - j6.9$
3.30	$2.8 - j5.1$	$2.0 - j6.6$
3.40	$2.7 - j4.6$	$2.0 - j6.2$
3.50	$2.3 - j3.8$	$1.9 - j6.0$
Impedance Definition		

PACKAGE DIMENSIONAL OUTLINE DRAWING



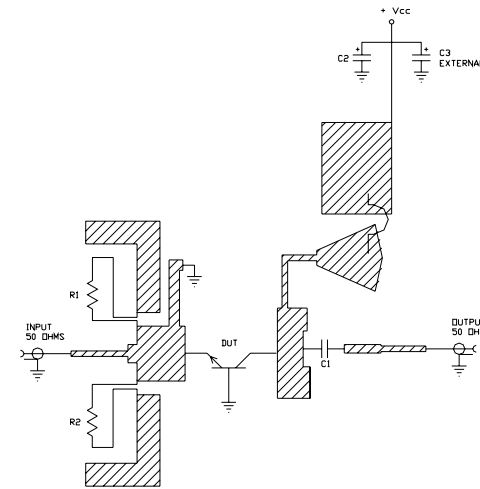
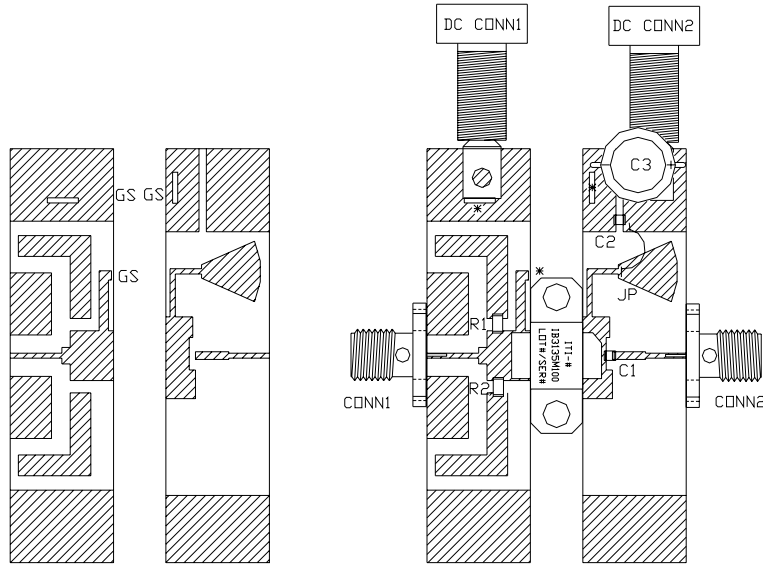
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.243	0.253	6.17	6.43
B	0.055	0.065	1.40	1.65
C	0.739	0.749	18.77	19.02
D	0.178	0.188	4.52	4.78
E	0.125	0.135	3.18	3.43
F	0.555	0.565	14.10	14.35
G	0.082	0.092	2.08	2.34
H	0.080	0.120	2.03	3.05
I	0.080	0.120	2.03	3.05
J	0.004	0.006	0.10	0.15
K	0.215	0.225	5.46	5.72
L	0.245	0.255	6.22	6.48
M	0.315	0.325	8.00	8.26

PIN SCHEDULE	
1	BASE
2	EMITTER
3	COLLECTOR

NOTICE TO PERSONS RECEIVING THIS DRAWING, INTEGRA TECHNOLOGIES, INC. CLAIMS PROPRIETARY RIGHTS IN THE MATERIAL DISCLOSED HEREON. THIS DRAWING MAY NOT BE REPRODUCED NOR MAY IT BE USED TO MANUFACTURE ANYTHING SHOWN HEREON WITHOUT THE WRITTEN PERMISSION OF INTEGRA TECHNOLOGIES, INC.

DOCUMENT NUMBER: IB3135M100	REV: PR1
SHEET NAME: 06-OUTLINE	REV: NC

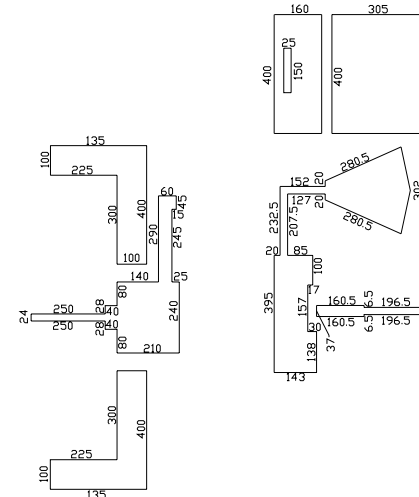
BROADBAND RF TEST FIXTURE



ELECTRICAL SCHEMATIC

COMPONENT	DESCRIPTION
DUT	TRANSISTOR #IB3135M100, MOUNT HARD TO THE RIGHT
PC BOARD	ROGERS #RT6010.2LM, TH=0.025" 2E/2E
C1, C2	CHIP CAPACITOR, TYPE ATC100A, 39 pF
C3	ELECTROLYTIC CAPACITOR, 68uF / 63V
C4 - NOT SHOWN	ELECTROLYTIC CAPACITOR, 2200uF / 63V
GS	GROUND SHIM, COPPER, TH=0.001"
CONN1, CONN2	SMA CONNECTOR, TYPE OS #2052-5636-02
INPUT PC BOARD CARRIER	0.5 INCH BRASS - 01
OUTPUT PC BOARD CARRIER	0.5 INCH BRASS - 01
TRANSISTOR CARRIER	2 INCH COPPER - 01
TRANSISTOR CLAMP	NORYL CLAMP -01
HEAT SINK	2 INCH HEAT SINK - 09
DC CONN1	BANANA JACK, BLACK
DC CONN2	BANANA JACK, RED
R1	51 ohm CHIP RESISTOR MSI # WA57PS-51RJ-NS62
R2	51 ohm CHIP RESISTOR MSI # WA57PS-51RJ-NS62
JP	JUMPER WIRE
NOTE	FIXTURE HARDWARE DRAWINGS AVAILABLE ON REQUEST

ASSEMBLY AND PARTS LIST



CIRCUIT DIMENSIONS IN MILS (1 MIL = 0.001")

DEFINITIONS

Data Sheet Status	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
Maximum Ratings	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only and operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

WARNING

Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO base is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with general or domestic waste.

DISCLAIMER

Integra Technologies Inc. makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Integra Technologies Inc. assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. Integra Technologies Inc. products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Integra Technologies Inc. customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Integra Technologies Inc. for any damages resulting from such improper use or sale.
--