

## S-Band Radar Transistor

The high power pulsed radar transistor device part number IB3135MH45 is designed for S-Band radar systems operating over the instantaneous bandwidth of 3.1-3.5 GHz. While operating in class C mode this common base device supplies a minimum of 45 watts of peak pulse power under the conditions of 100 $\mu$ s pulse width and 10% duty cycle over the frequency range of 3.1-3.5 GHz. All devices are 100% screened for large signal RF parameters, including power gain compression. Excellent spectral stability into output mismatch over a broad input power range make it ideal for use in reliable high power solid state transmitters. The test fixture includes a passive amplitude sloping network to insure that the device is not overdriven as the operating frequency decreases. This device is rated for a peak output power level of  $P_{PEAK} = 45W @ 10\%$  duty factor. This corresponds to an average power  $P_{AVG} = 4.5W$ .



- Silicon Bipolar
  - Ultra-high  $f_T$
- Class C Operation
  - High Efficiency
- Common Base Configuration
  - Single Power Supply
- Gold Metal
  - Maximum Reliability
- Emitter Ballasting
  - Optimum Thermal Distribution
- Internal Impedance Matching
  - Ease of Use
  - Ultra-low Loss Design
- BeO Package
  - Unmatched Thermal Reliability
  - Solder Seal Hermeticity
- RF Test Fixture
  - Broadband
  - Matched to 50 $\Omega$
  - Long-term Correlation
  - 100% Device RF Screening
  - No External Tuning Allowed
- Insertion Phase Marking
  - 5 $^\circ$  Increment Marking
- US Patent Number
  - US 6181200B1
  - US 6331931B1
  - US 8344809B2

**TYPICAL DATA    TYPICAL DATA    TYPICAL DATA    TYPICAL DATA**

Freq (MHz)	PW (us)	Duty (%)	V <sub>CC</sub> (V)	P <sub>IN</sub> (W)	IRL (dB)	P <sub>OUT</sub> (W)	G <sub>P</sub> (dB)	I <sub>C</sub> (A)	N <sub>C</sub> (%)	Droop (dB)
3.100	100	10	36.0	6.5	-15	66	10.1	4.17	44	-0.40
3.200	100	10	36.0	6.5	-16	62	9.8	4.15	41	-0.40
3.300	100	10	36.0	6.5	-18	59	9.6	6.94	42	-0.30
3.400	100	10	36.0	6.5	-18	57	9.4	4.01	39	-0.40
3.500	100	10	36.0	6.5	-15	52	9.1	3.73	39	-0.10

**MAXIMUM RATINGS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Collector-Emitter Voltage	$V_{CES}$	--	70	V	$V_{BE}=0V$ .
BD	Storage Temperature Range	$T_{STG}$	-65	+200	°C	--
BD	Operating Junction Temperature Range	$T_J$	-55	+200	°C	--
BD	CW Operation	--	--	--	--	Not rated for CW operation.
Note	Screen 'BD' = parameter qualified By Design.					

**THERMAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	0.70	°C/W	$V_{CC}=V1$ , $PW=PW1$ , $DF=DF1$ , $T_F=25\pm5^\circ C$ , $P_{OUT}=45W$ , $N_C=38\%$ .
BD	Mean Time To Failure	MTTF	2.34E10	--	Hrs	$V_{CC}=V1$ , $PW=PW1$ , $DF=DF1$ , $T_F=25\pm5^\circ C$ , $P_{OUT}=45W$ , $N_C=38\%$ .
Note	GB = Guard Band. Screen 'BD' = parameter qualified By Design.					

**PROCESSING SPECIFICATIONS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071.6, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

**DC ELECTRICAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Collector-Emitter Breakdown Voltage	$BV_{CES}$	70	--	V	$I_C=15mA$ , $V_{BE}=0V$ , $T_F=25\pm5^\circ C$ .
100%	Zero Base Voltage Collector Leakage Current	$I_{CES}$	--	3.0	mA	$V_{CE}=30V$ , $V_{BE}=0V$ , $T_F=25\pm5^\circ C$ .
100%	DC Current Gain	$H_{FE}$	10	120	--	$V_{CE}=5V$ , $I_C=0.1A$ , $T_F=25\pm5^\circ C$ .

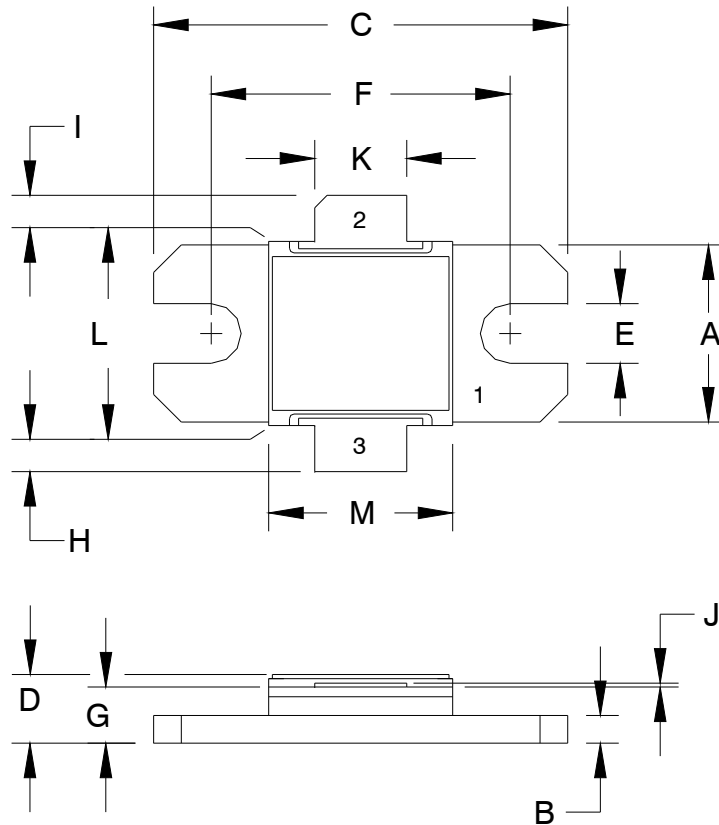
**RF ELECTRICAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	IRL1	8	--	dB	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, F=F1.$
100%	Input Return Loss	IRL2	9	--	dB	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN2}, F=F2.$
100%	Input Return Loss	IRL3	10	--	dB	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN3}, F=F3.$
100%	Output Power	$P_{O1}$	45	--	W	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, F=F1.$
100%	Output Power	$P_{O2}$	45	--	W	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN2}, F=F2.$
100%	Output Power	$P_{O3}$	45	--	W	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN3}, F=F3.$
100%	Collector Efficiency ( $P_O/I_C/V_{CC}$ )	$N_{C1}$	36	--	%	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, F=F1.$
100%	Collector Efficiency ( $P_O/I_C/V_{CC}$ )	$N_{C2}$	36	--	%	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN2}, F=F2.$
100%	Collector Efficiency ( $P_O/I_C/V_{CC}$ )	$N_{C3}$	36	--	%	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN3}, F=F3.$
100%	Pulse Amplitude Droop	D1	--	0.8	dB	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, F=F1.$
100%	Pulse Amplitude Droop	D2	--	0.8	dB	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN2}, F=F2.$
100%	Pulse Amplitude Droop	D3	--	0.8	dB	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN3}, F=F3.$
100%	Output Power Compression = $10*\text{LOG}(P_{OC}/P_O)$	OPC1	+0.02	+0.48	dB	$P_{OC}$ measured with $P_{IN}$ increased by 0.5dB at $F=F1.$
100%	Output Power Compression = $10*\text{LOG}(P_{OC}/P_O)$	OPC2	+0.02	+0.48	dB	$P_{OC}$ measured with $P_{IN}$ increased by 0.5dB at $F=F2.$
100%	Output Power Compression = $10*\text{LOG}(P_{OC}/P_O)$	OPC3	+0.02	+0.48	dB	$P_{OC}$ measured with $P_{IN}$ increased by 0.5dB at $F=F3.$
100%	Output Power Flatness = $10*\text{LOG}(P_{OMAX}/P_{OMIN})$	OPF	--	1.5	dB	Calculate from $P_O$ at each frequency $F.$
100%	Delta Insertion Phase Variation	d-IP	-30	+30	Deg	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN3}, F=F3,$ Mark in $5^\circ$ increments.
100%	Stability into 1.5:1 VSWR with +0.75dB overdrive	VSWR-S	--	--	--	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, P_{IN2}, P_{IN3}, F=F1, F2, F3.$ Repeat $P_O$ with $P_{IN}$ increased by 0.75dB. Rotate 1.5:1 output VSWR through $360^\circ$ phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse. All non-harmonically related signals must be at least -65 dBc.
100%	2:1 Load Mismatch Tolerance	LMT	--	--	--	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, P_{IN2}, P_{IN3}, F=F1, F2, F3.$ Rotate 2:1 output VSWR through $360^\circ$ phase. Post test $P_O = \text{Pre test } P_O \pm 3W.$
Note	$V1 = 36V; PW1 = 100\mu s; DF1 = 10%; P_{IN1} = P_{IN2} = P_{IN3} = 6.5W; F1 = 3.30 \text{ GHz}, F2 = 3.20 \text{ GHz}, F3 = 3.50 \text{ GHz}.$					
Note	$T_F = \text{Device flange temperature. Screen 'BD' = parameter qualified By Design.}$					
Note	Parts are binned and marked in 5 degree increments for Insertion Phase IP : ITI-1, -2, -3, -4, -5, -6, -7, -8, -9, -10, -11, -12.					

**RF TEST FIXTURE IMPEDANCE CHARACTERISTICS**

Frequency (MHz)	$Z_{IF}$ ( $\Omega$ )	$Z_{OF}$ ( $\Omega$ )
3.10	7.0 -j8.6	5.0 -j7.4
3.20	6.7 -j8.6	4.7 -j7.1
3.30	6.0 -j8.4	4.5 -j6.7
3.40	5.4 -j8.2	4.3 -j6.4
3.50	4.6 -j7.7	4.1 -j6.1
Impedance Definition		

**PACKAGE DIMENSIONAL OUTLINE DRAWING**



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.380	0.390	9.65	9.91
B	0.058	0.062	1.47	1.57
C	0.895	0.905	22.73	22.99
D	0.157	0.177	3.99	4.50
E	0.125	0.135	3.18	3.43
F	0.645	0.655	16.38	16.64
G	0.112	0.132	2.84	3.35
H	0.035	0.105	0.89	1.91
I	0.035	0.105	0.89	2.67
J	0.003	0.005	0.08	0.13
K	0.195	0.205	4.95	5.21
L	0.395	0.405	10.03	10.29
M	0.395	0.405	10.03	10.29

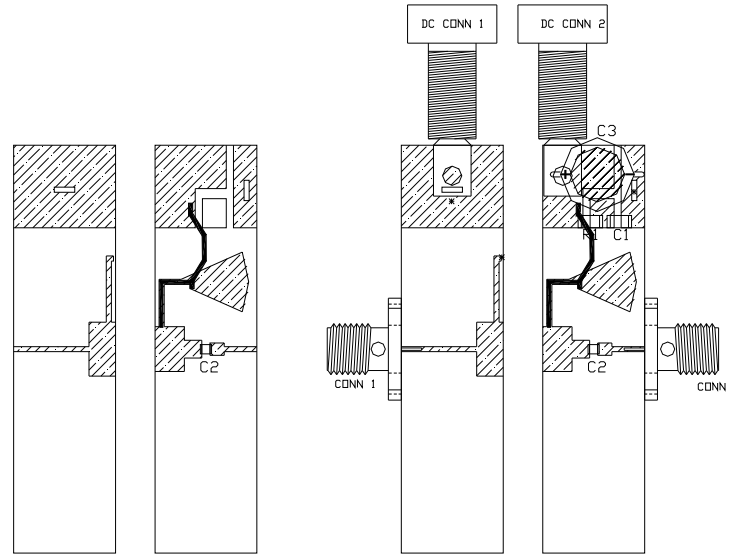
PIN	
1	BASE
2	COLLECTOR
3	EMITTER

NOTES:

LID: LID-P44-1

FLANGE: F900385A1

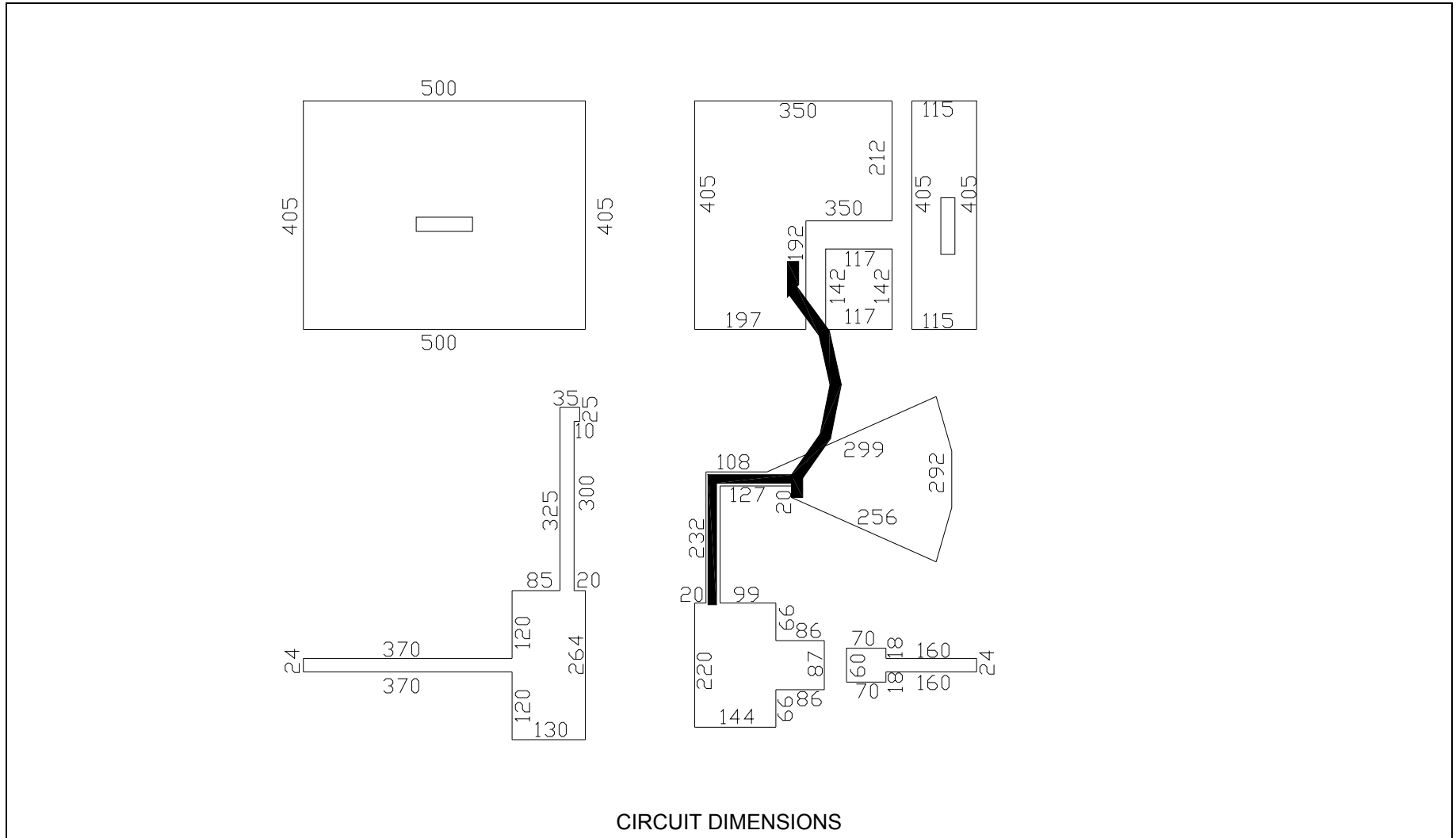
**RF TEST FIXTURE**



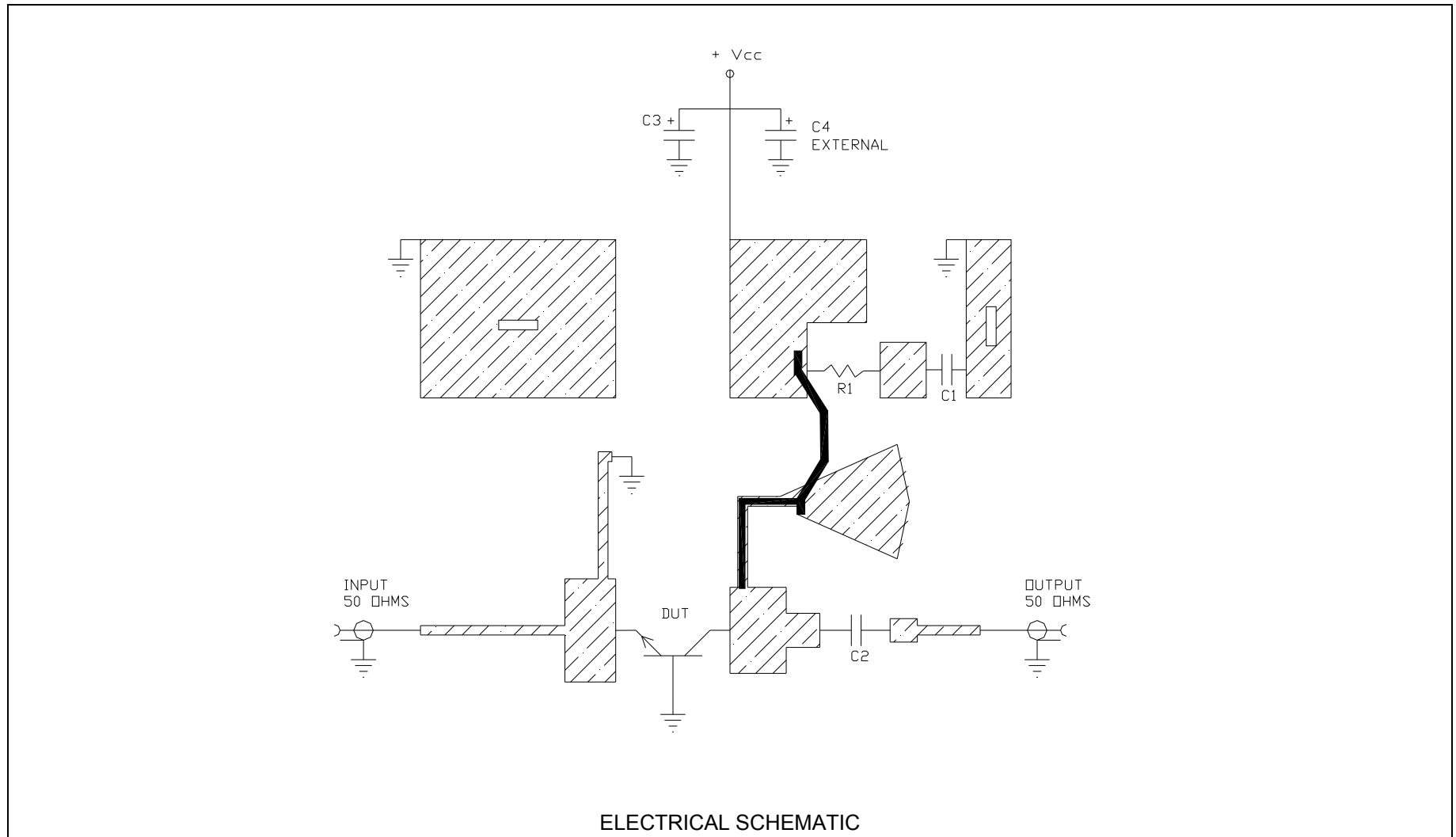
COMPONENT	DESCRIPTION
DUT	TRANSISTOR #IB3135MH45, MOUNT HARD TO THE RIGHT
PC BOARD	ROGERS #R06010.5LM, TH=0.025" 1oz. Cu BOTH SIDES
C1	SNUB CAPACITOR 1uF
C2	CHIP CAPACITOR, TYPE ATC100A, 39 pF
C3	ELECTROLYTIC CAPACITOR, 68uF / 63V
C4 - NOT SHOWN	ELECTROLYTIC CAPACITOR, 2200uF / 63V
R1	SNUB RESISTOR 6.810HMS
GS	GROUND SHIM, COPPER, TH=0.001"
CONN1, CONN2	SMA CONNECTOR, TYPE QS #2052-5636-02
INPUT PC BOARD CARRIER	0.50 INCH BRASS - 01
OUTPUT PC BOARD CARRIER	0.50 INCH BRASS - 01
TRANSISTOR CARRIER	2 INCH COPPER - 02 (P44)
TRANSISTOR CLAMP	NDRYL CLAMP -03 (P44)
HEATSINK	2 INCH HEATSINK - 09
DC CONN1	BANANA JACK, BLACK
DC CONN2	BANANA JACK, RED
JP	JUMPER WIRE, 1 PLACE
NOTE	FIXTURE HARDWARE DRAWINGS AVAILABLE ON REQUEST

**ASSEMBLY AND PARTS LIST**

**RF TEST FIXTURE**



**RF TEST FIXTURE**



**ELECTRICAL SCHEMATIC**



**DEFINITIONS**

<b>Data Sheet Status</b>	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
<b>Maximum Ratings</b>	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only. Operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

**WARNING**

<b>Product and environmental safety - toxic materials</b>
This product contains beryllium oxide. The product is entirely safe provided that the BeO base is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with general or domestic waste.

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