Part Number: IGN0912LM500

Integra
TECHNOLOGIES, INC.

L-Band Avionics Transistor - GaN

- GaN on SiC HEMT Technology
- P_{OUT-PK} ≥ 500W @ 48 X 32uS ON, 18us OFF/ 6.4% DC / 50V
- 0.96-1.22GHz Instantaneous Operating Frequency Range
- Internal Impedance Pre-matched Device
- Depletion Mode Device
- Negative Gate Voltage and Bias Sequencing Required
- Specified For Use Under Class AB Operation
- Metal Based Package Sealed With Ceramic-Epoxy Lid
- Gold Metallization System: Chip - Wire Bond - Package
- Package Size: W=0.800″ (20.032mm), L=0.400″ (10.16mm)
- 100% High Power RF Tested in Broadband RF Test Fixture

PARAMETER	SYM	MIN	TYP	MAX	UNITS	TEST CONDITIONS
DC ELECTRICAL SPECIFICATIONS						
Drain Leakage Current	I_{D-OFF}	--	--	2.0	mA	V_{DS}=50V, V_{GS}=-6V, T_{F1}, S1
Gate Threshold Voltage	V_{GS-TH}	--	-2.6	--	V	V_{DS}=50V, I_D=100mA, T_{F1}, BD
RF ELECTRICAL SPECIFICATIONS						
Input Return Loss	IRL	-18	-12	-7	dB	PO1, V1, I_{DQ1}, PW1, DF1, F1, F2, F3, T_{F1}, S1
Input Power	PIN	6.3	8.0	11.0	W	PO1, V1, I_{DQ1}, PW1, DF1, F1, F2, F3, T_{F1}, S1
Power Gain	Gp	16.6	18.0	19.0	dB	PO1, V1, I_{DQ1}, PW1, DF1, F1, F2, F3, T_{F1}, S1
Drain Efficiency	N_D	50	60	75	%	PO1, V1, I_{DQ1}, PW1, DF1, F1, F2, F3, T_{F1}, S1
Pulse Amplitude Droop	D	-0.5	-0.2	+0.2	dB	PO1, V1, I_{DQ1}, PW1, DF1, F1, F2, F3, T_{F1}, S1
Load Mismatch Stability	VSWR-S	2:1	--	--	--	PO1, V1, I_{DQ1}, PW1, DF1, F1, F2, F3, T_{F1}, S1
Load Mismatch Tolerance	LMT	3:1	--	--	--	PO1, V1, I_{DQ1}, PW1, DF1, F1, F2, F3, T_{F1}, S1

DC & RF TEST CONDITIONS	SYM	MIN	NOM	MAX	UNITS	NOTES
Output Power 1	PO1	--	500	--	W	--
Drain Supply Voltage 1	V1	--	50	--	V	--
Quiescent Drain Current 1	I_{DQ1}	70	75	80	mA	--
Pulse Width 1	PW1	--	*	--	us	* Pulse Train - 48 X 32uS ON, 18uS OFF
Duty Factor 1	DF1	--	6.4	--	%	--
Frequency 1	F1	--	0.960	--	GHz	--
Frequency 2	F3	--	1.090	--	GHz	
Frequency 3	F5	--	1.220	--	GHz	--
Flange Temperature 1	T_{F1}	25	30	35	°C	--
Screening Level 1	S1	--	100	--	%	--

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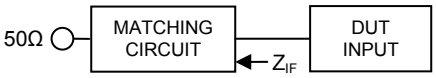
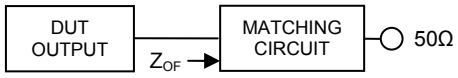
PARAMETER	SYM	MIN	MAX	UNITS	SCREEN	CONDITIONS
MAXIMUM RATINGS						
Drain-Source Voltage	V_{DS}	--	160	V	BD	T_F = 25°C
Gate-Source Voltage	V_{GS}	-10	0	V	BD	T_F = 25°C
Storage Temperature Range	T_{STG}	-55	+150	°C	BD	--
Operating Junction Temperature	T_J	-55	+200	°C	BD	--
PROCESS SPECIFICATIONS						
DC Wafer Probe	--	--	--	--	100%	Per Integra Spec
Wafer DC, RF Qualification	--	--	--	--	Q1	Per Integra Spec
Wire Bond Strength	--	--	--	--	LM	Per Integra Spec
Pre-cap Visual Inspection	--	--	--	--	100%	Per Integra Spec
Gross Leak Test – MIL-STD-750D	--	--	--	--	100%	Method 1071.6 C
THERMAL RESISTANCE						
Peak Thermal Resistance Per Rated RF Specification	$R_{TH(JC)}$	--	0.27	°C/W	BD	T_F = 25°C
SCREENING LEVELS						
Parameter Qualified By Design	BD	--	--	--	--	--
Parameter Qualified By 3 Pieces (min) Per Wafer	Q1	--	--	--	--	--
Parameter Qualified By Assembly Line Monitor	LM	--	--	--	--	--

RF TEST FIXTURE – BROADBAND

► Broadband RF Test Fixture. Provides Device Impedance Matching to 50Ω Across the Rated Operating Frequency Range.

► Electronic CAD Drawing File Available Upon Request. Includes Circuit Dimensions and Parts List.

► Reference Design PCB: Rogers RTD6006-02511, DK=6.15.

FREQUENCY (GHz)	Z_{IF}(Ω)	Z_{OF}(Ω)
0.96	6.1 – j 2.4	1.8 + j 0.1
1.09	6.2 – j 0.5	2.0 + j 0.1
1.22	6.9 – j 1.2	1.6 + j 0.1
Impedance Definition		

DC BIAS SEQUENCING

Turn ON GaN Device	Turn OFF GaN Device
1. RF Power OFF 2. Set VGS = -5V (Negative Voltage to pinch off) 3. Measure VDS impedance, should be pinched off. 4. Turn ON VDD voltage. 5. Slowly increase VGS until bias current IDQ is set. 6. Turn ON RF Power	1. Turn OFF RF Power 2. Turn OFF VDD voltage 3. After VDD is discharged, set VGS = -5V 4. Turn OFF VGS voltage.

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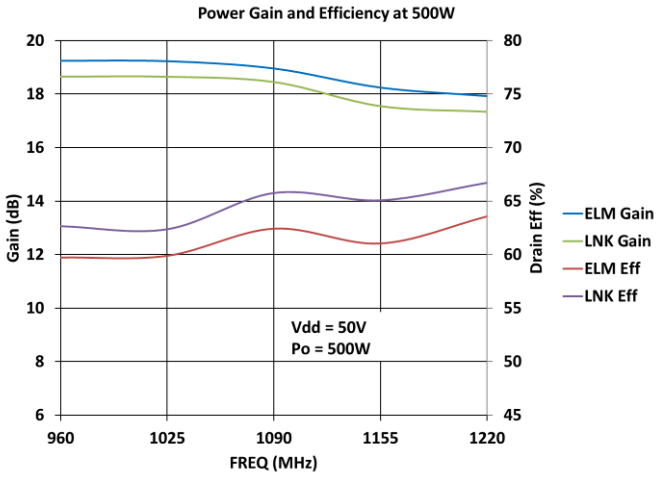
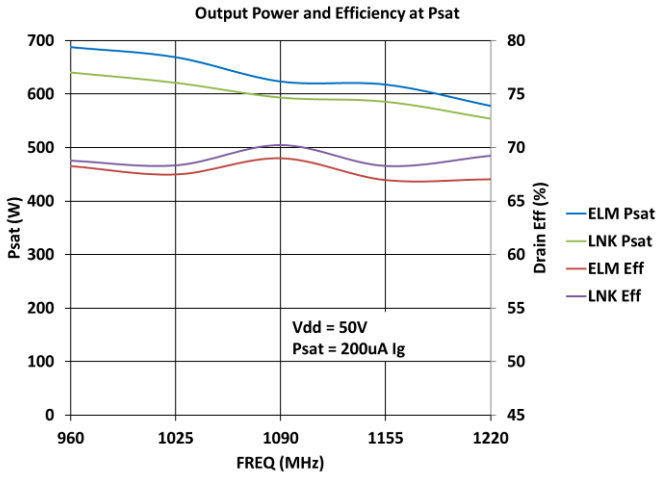
TYPICAL PERFORMANCE





Waveform Definition:
ELM = Pulse Train 48X 32us on 18us off, 6.4% Duty Cycle
LNK = Pulse Train 444X 7us on 6us off, 22.7% Duty Cycle

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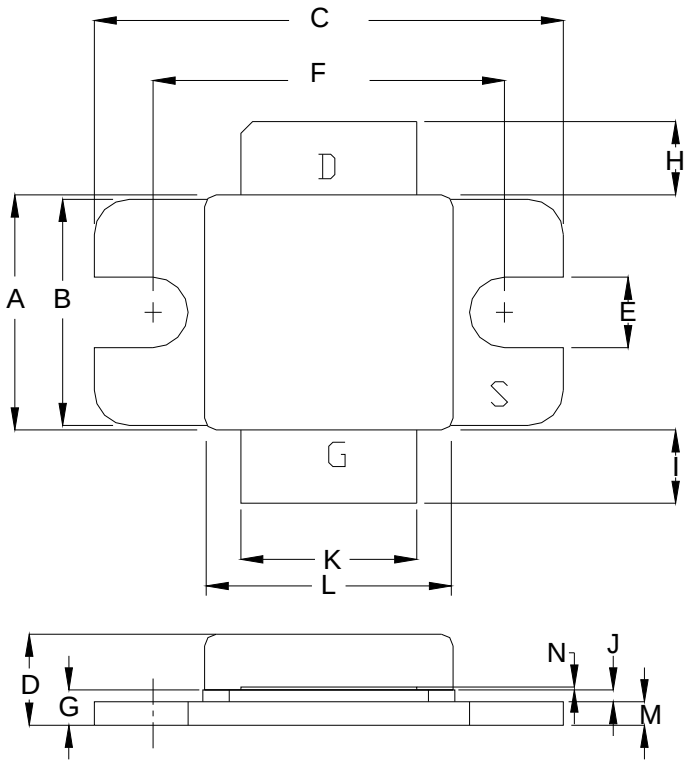
PACKAGE OUTLINE DRAWING



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.395	0.405	10.03	10.29
B	0.380	0.390	9.65	9.91
C	0.795	0.805	20.19	20.45
D	0.143	0.177	3.63	4.49
E	0.115	0.125	2.92	3.17
F	0.595	0.605	15.11	15.37
G	0.053	0.065	1.35	1.65
H	0.110	0.140	0.28	0.36
I	0.110	0.140	0.28	0.36
J	0.018	0.022	0.046	0.056
K	0.295	0.305	7.49	7.74
L	0.425	0.435	10.80	11.05
M	0.035	0.045	0.89	1.14
N	0.004	0.007	0.10	0.17

PIN SCHEDULE	
D	DRAIN
S	SOURCE
G	GATE

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DEFINITIONS	
DATA SHEET STATUS	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
MAXIMUM RATINGS	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

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