L-Band Radar Transistor - GaN

- GaN on SiC HEMT Technology
- $P_{OUT-PK} \geq$ 500W @ 2.0ms / 20% / 50V
- 1.2-1.4GHz Instantaneous Operating Frequency Range
- Internal Impedance Pre-matched Device
- Depletion Mode Device
- Negative Gate Voltage and Bias Sequencing Required
- Specified For Use Under Class AB Operation
- Metal Based Package Sealed With Ceramic-Epoxy Lid
- Gold Metallization System: Chip - Wire Bond - Package
- Package Size: W=1.176″ (29.87mm), L=0.540″ (13.72mm)
- 100% High Power RF Tested in Broadband RF Test Fixture

PARAMETER	SYM	MIN	TYP	MAX	UNITS	TEST CONDITIONS
DC ELECTRICAL SPECIFICATIONS						
Drain Leakage Current	I_{D-OFF}	--	--	4.0	mA	V_{DS}=50V, V_{GS}=-6V, T_{F1}, S1
Gate Threshold Voltage	V_{GS-TH}	--	-2.8	--	V	V_{DS}=50V, I_D=100mA, T_{F1}, BD
RF ELECTRICAL SPECIFICATIONS						
Input Return Loss	IRL	-18	-15	-7	dB	PO1, V1, I_{DQ1}, PW1, DF1, F1, F2, F3, T_{F1}, S1
Input Output	PIN	11.2	16.0	17.5	W	PO1, V1, I_{DQ1}, PW1, DF1, F1, F2, F3, T_{F1}, S1
Power Gain	Gp	14.5	15.0	16.5	dB	PO1, V1, I_{DQ1}, PW1, DF1, F1, F2, F3, T_{F1}, S1
Drain Efficiency	N_D	52	65	75	%	PO1, V1, I_{DQ1}, PW1, DF1, F1, F2, F3, T_{F1}, S1
Pulse Amplitude Droop	D	-0.8	-0.4	+0.10	dB	PO1, V1, I_{DQ1}, PW1, DF1, F1, F2, F3, T_{F1}, S1
Load Mismatch Stability	VSWR-S	2:1	--	--	--	PO1, V1, I_{DQ1}, PW1, DF1, F1, F2, F3, T_{F1}, S1
Load Mismatch Tolerance	LMT	3:1	--	--	--	PO1, V1, I_{DQ1}, PW1, DF1, F1, F2, F3, T_{F1}, S1

DC & RF TEST CONDITIONS	SYM	MIN	NOM	MAX	UNITS	TEST CONDITIONS
Output Power 1	PO1	--	500	--	W	--
Drain Supply Voltage 1	V1	--	50	--	V	--
Quiescent Drain Current 1	I_{DQ1}	--	200	--	mA	--
Pulse Width 1	PW1	--	2.0	--	ms	--
Duty Factor 1	DF1	--	20	--	%	--
Frequency 1	F1	1.20	1.20	1.20	GHz	--
Frequency 2	F2	1.30	1.30	1.30	GHz	--
Frequency 3	F3	1.40	1.40	1.40	GHz	--
Flange Temperature 1	T_{F1}	25	30	35	°C	--
Screening Level 1	S1	100	--	--	%	--

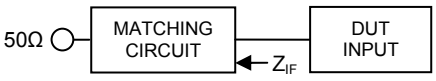
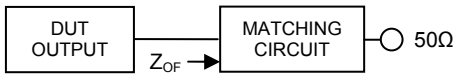
www.integratech.com
PHONE: 310-606-0855
FAX: 310-606-0865

INTEGRA TECHNOLOGIES, INC.
321 CORAL CIRCLE
EL SEGUNDO, CA 90245-4620

PARAMETER	SYM	MIN	MAX	UNITS	SCREEN	CONDITIONS
MAXIMUM RATINGS						
Drain-Source Voltage	V_{DS}	--	160	V	BD	T_F = 25°C
Gate-Source Voltage	V_{GS}	-10	0	V	BD	T_F = 25°C
Storage Temperature Range	T_{STG}	-55	+150	°C	BD	--
Operating Junction Temperature	T_J	-55	+200	°C	BD	--
PROCESS SPECIFICATIONS						
DC Wafer Probe	--	--	--	--	100%	Per Integra Spec
Wafer DC, RF Qualification	--	--	--	--	Q1	Per Integra Spec
Wire Bond Strength	--	--	--	--	LM	Per Integra Spec
Pre-cap Visual Inspection	--	--	--	--	100%	Per Integra Spec
Gross Leak Test – MIL-STD-750D	--	--	--	--	100%	Method 1071.6 C
THERMAL RESISTANCE						
Peak Thermal Resistance Per Rated RF Specification	$R_{TH(JC)}$	--	0.22	°C/W	BD	T_F = 25°C
SCREENING LEVELS						
Parameter Qualified By Design	BD	--	--	--	--	--
Parameter Qualified By 3 Pieces (min) Per Wafer	Q1	--	--	--	--	--
Parameter Qualified By Assembly Line Monitor	LM	--	--	--	--	--

RF TEST FIXTURE – BROADBAND

- ► Broadband RF Test Fixture. Provides Device Impedance Matching to 50Ω Across the Rated Operating Frequency Range.
- ► Electronic CAD Drawing File Available Upon Request. Includes Circuit Dimensions and Parts List.
- ► Reference Design PCB: Rogers 6010.2 – 0.025" – 1/1

FREQUENCY (GHz)	Z_{IF}(Ω)	Z_{OF}(Ω)
1.20	1.8 – j 1.1	2.0 – j 1.8
1.30	2.0 – j 0.3	2.0 – j 1.6
1.40	2.3 + j 0.4	1.9 – j 1.4
Impedance Definition		

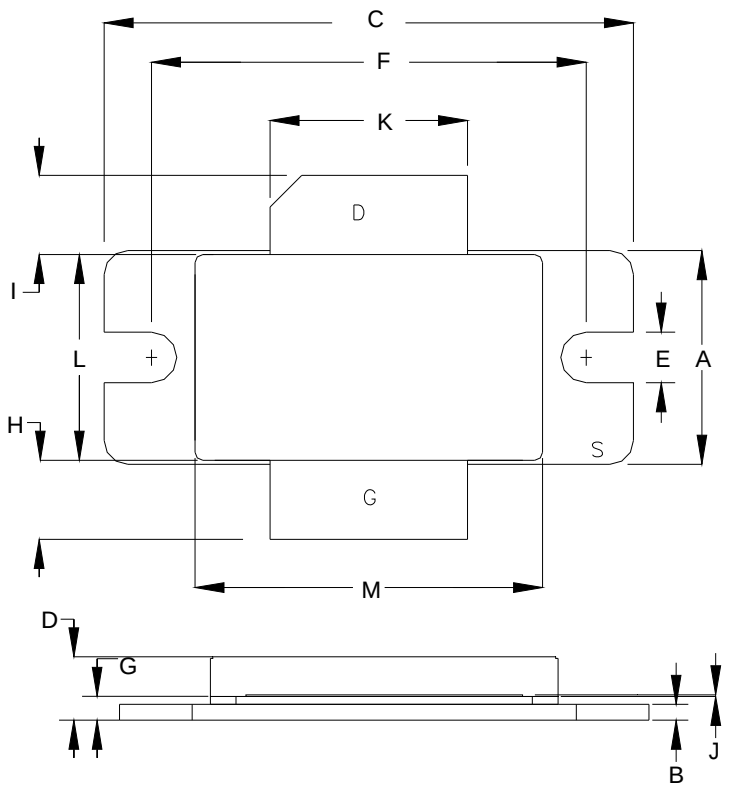
DC BIAS SEQUENCING

Turn ON GaN Device	Turn OFF GaN Device
1. RF Power OFF 2. Set VGS = -5V (Negative Voltage to pinch off) 3. Turn ON VDD voltage. 4. Slowly increase VGS until bias current IDQ is set. 5. Turn ON RF Power	1. Turn OFF RF Power 2. Turn OFF VDD voltage 3. After VDD is discharged, set VGS = -5V 4. Turn OFF VGS voltage.

www.integratech.com
PHONE: 310-606-0855
FAX: 310-606-0865

INTEGRA TECHNOLOGIES, INC.
321 CORAL CIRCLE
EL SEGUNDO, CA 90245-4620

PACKAGE OUTLINE DRAWING



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.535	0.545	13.59	13.84
B	0.035	0.045	0.89	1.14
C	1.335	1.345	33.91	34.16
D	0.145	0.187	3.68	4.75
E	0.123	0.133	3.12	3.38
F	1.095	1.105	27.81	28.07
G	0.059	0.065	1.50	1.65
H	0.170	0.210	4.32	5.33
I	0.170	0.210	4.32	5.33
J	0.003	0.006	0.08	0.15
K	0.495	0.505	12.57	12.83
L	0.515	0.525	13.08	13.34
M	0.871	0.889	22.12	22.58

PIN SCHEDULE	
D	DRAIN
S	SOURCE
G	GATE

www.integratech.com
PHONE: 310-606-0855
FAX: 310-606-0865

INTEGRA TECHNOLOGIES, INC.
321 CORAL CIRCLE
EL SEGUNDO, CA 90245-4620

DEFINITIONS	
DATA SHEET STATUS	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
MAXIMUM RATINGS	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

DISCLAIMER

Integra Technologies Inc. makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Integra Technologies Inc. assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. Integra Technologies Inc. products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Integra Technologies Inc. customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Integra Technologies Inc. for any damages resulting from such improper use or sale.

www.integratech.com
PHONE: 310-606-0855
FAX: 310-606-0865

INTEGRA TECHNOLOGIES, INC.
321 CORAL CIRCLE
EL SEGUNDO, CA 90245-4620