

S-Band Radar Transistor

IGN2729M400 is an internally pre-matched, gallium nitride (GaN) high electron mobility transistor (HEMT). This part is designed for S-Band radar applications operating over the 2.7 – 2.9 GHz instantaneous frequency band. Under 300us / 10% pulse conditions it supplies a minimum of 400 watts of peak output power with 11dB gain typically. Specified operation is with Class AB bias. When appropriately rated, it is operable under a wide range of pulse widths and duty factors. All devices are 100% screened for large signal RF parameters in a fixed tuned broadband matching circuit / test fixture. The use of external tuners is not allowed during screening. This device is rated for a peak output power level of $P_{PEAK} = 400W$ @ 10% duty factor. This corresponds to an average power $P_{AVG} = 40W$.



GaN on Silicon Carbide FET

- High Power Gain
- Excellent thermal stability
- Gold Metal

Depletion Mode Device

- Negative Gate Voltage to Bias
- Bias Sequencing Required
- See App Note to Prevent Damage

Gold Metal System

- Complete Gold System
- Gold Bond Wires
- Gold Package Metal
- Maximum Reliability

Class AB Operation

- Specified with AB bias

Internal Impedance Matching

- Ease of Use
- Ultra Low Loss Design

BeO Free Package

- Metal Based
- Epoxy Seal

High Power RF Test / Fixture

- Broadband
- Matched to 50 Ω (ohms)
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning required

SAMPLE RF DATA IN BROADBAND RF TEST FIXTURE

Lot/SN:	F (GHz)	Pi (W)	Id (A)	RL (dB)	Po (W)	Nd (%)	G (dB)	Drp (dB)	VSWR 3:1
50023928-1	2.7	34	15.15	12	434	57.3	11.06	-0.23	P
	2.8	34	16.26	18	472	58.1	11.42	-0.23	P
	2.9	34	16.40	15	459	56.0	11.30	-0.22	P

Vd=50V, Idq=100mA, Pulse 300us/10%

MAXIMUM RATINGS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Drain-Source Voltage	V_{DS}	--	60	V	--
BD	Gate-Source Voltage	V_{GS}	-10	0	V	--
BD	Storage Temperature Range	T_{STG}	-55	+150	°C	--
BD	Operating Junction Temperature Range	T_J	-55	+200	°C	--
BD	CW Operation	--	--	--	--	Not rated for CW operation.
Note	Screen 'BD' = parameter qualified By Design.					

THERMAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	0.19	°C/W	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=57°C, P_{OUT}=476W$
BD	Mean Time To Failure - Average	MTTF-Avg	--	8.0E8	Hours	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=80°C, P_{OUT}=450W, N_D=53%$
Note	Screen 'BD' = parameter qualified By Design.					

PROCESSING SPECIFICATIONS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071.6, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					


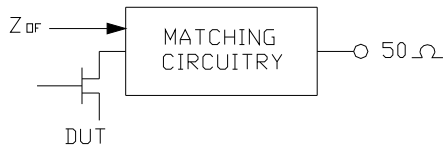
DC ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
100%	Drain Leakage Current	I_{D-OFF}	--	--	3.0	mA	$V_{DS} = 50V, V_{GS} = -6V, T_F = 25\pm5°C$
BD	Gate Threshold Voltage	V_{GS-TH}	--	-2.8	--	V	$V_{DS} = 50V, I_D = 100mA, T_F = 25\pm5°C$

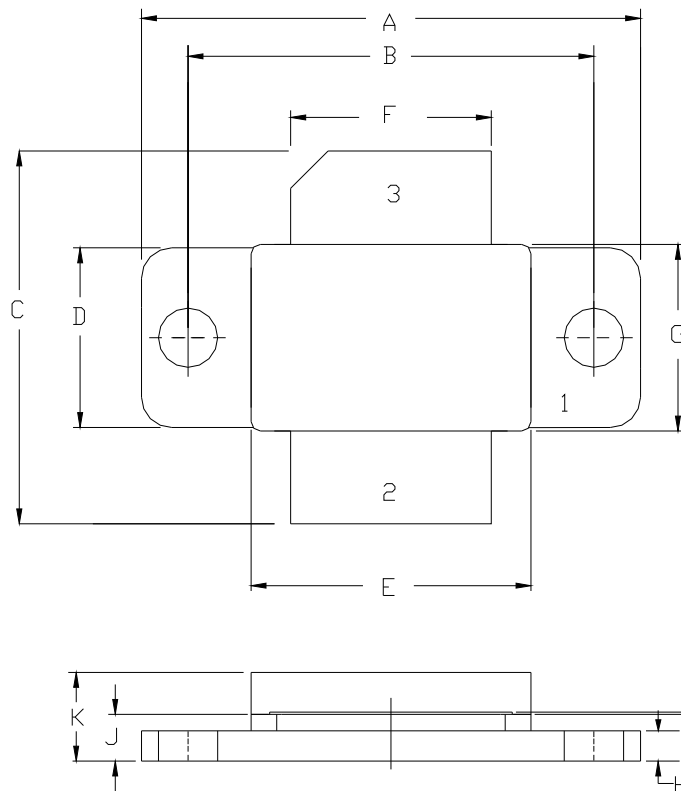
RF ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
100%	Input Return Loss	IRL	-18	-12	-9	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Output Power	P_O	400	440	634	W	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Power Gain	G_P	10.71	11.21	12.71	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Output Power Flatness $10^*LOG(P_{O-MAX}/P_{O-MIN})$	OPF	0	1.0	1.5	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Drain Efficiency	N_D	53	58	75	%	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Drain Current	I_D	10	16	24	A	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Pulse Amplitude Droop	D	-0.50	-0.25	0.30	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Insertion Phase	IP	-30	0	+30	deg	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F3.$
BD	Risetime-Falltime	RT-FT	--	--	60	ns	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	2:1 Load Mismatch Stability	VSWR-S	2:1	--	--	--	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$ Rotate 2:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse. All non-harmonically related signals must be at least -65 dBc.
100%	3:1 Load Mismatch Tolerance	LMT	3:1	--	--	--	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$ Rotate 3:1 output VSWR through 360° phase. Post test P_O = Pre test $P_{O\pm 5W}$
Note 1	$V1 = 50V; I_{DQ1} = 100mA; PW1 = 300us; DF1 = 10\%, P_{IN1} = 34W.$						
Note 2	Test Frequencies: F1 = 2.7GHz, F2 = 2.8GHz, F3 = 2.9GHz.						
Note 3	All devices are marked with delta insertion phase dash numbers, following the part number, from -1 thru -12 indicating 5° variations between -30° to +30° from reference.						
Note 4	$T_{F1} = 25\pm 5^{\circ}C$ = Device flange temperature.						
Note 5	Screen 'BD' = parameter qualified By Design.						

RF TEST FIXTURE IMPEDANCE CHARACTERISTICS

Frequency (GHz)	$Z_{IF} (\Omega)$	$Z_{OF} (\Omega)$
2.70	3.1 -j1.6	3.3 -j1.0
2.80	3.1 -j1.0	3.0 -j0.3
2.90	3.3 -j0.3	3.2 +j0.6
Impedance Definition		

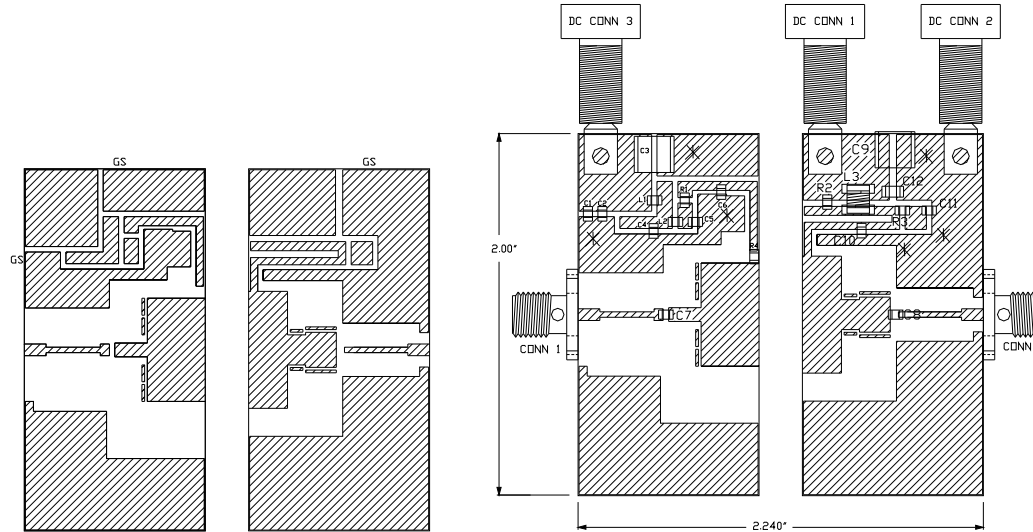
PACKAGE DIMENSIONAL OUTLINE DRAWING



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.065	1.075	27.05	27.30
B	0.865	0.875	21.97	22.22
C	0.794	0.804	20.17	20.42
D	0.380	0.390	9.65	9.90
E	0.595	0.605	15.11	15.37
F	0.425	0.435	10.79	11.05
G	0.395	0.405	10.03	10.29
H	0.060	0.070	1.52	1.78
I	0.004	0.006	0.10	0.15
J	0.096	0.106	2.44	2.69
K	0.184	0.196	4.67	4.98

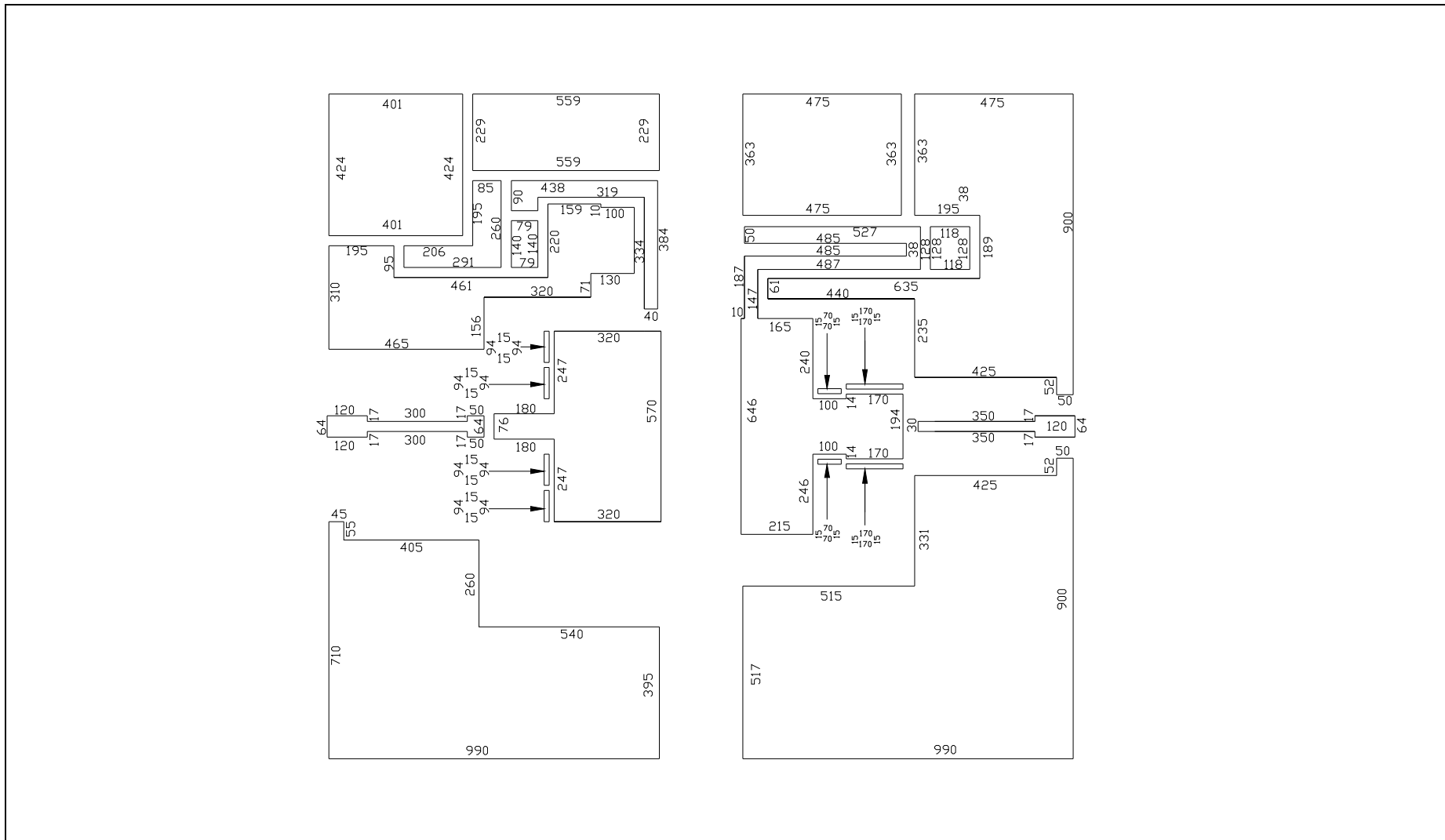
PIN SCHEDULE	
1	SOURCE
2	GATE
3	DRAIN

RF TEST FIXTURE

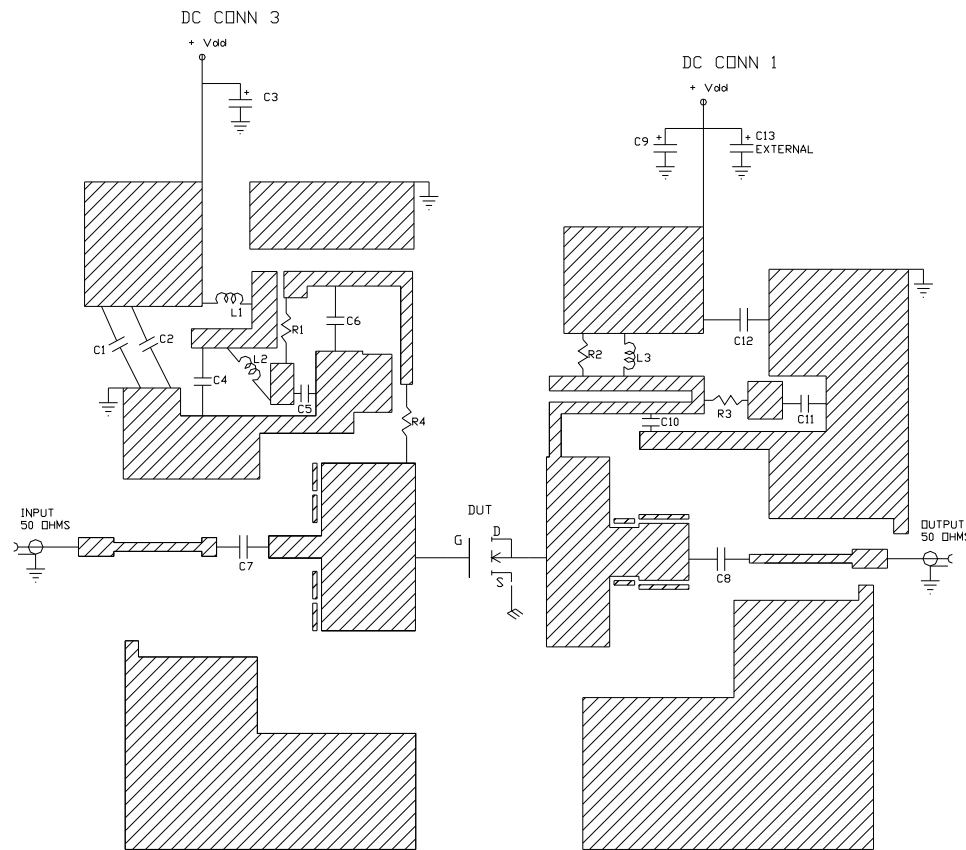


COMPONENT	DESCRIPTION
DUT	TRANSISTOR #IGN2729M400 MOUNT HARD TO THE RIGHT
PC BOARD	ROGERS #RD4350B-03011, 30MIL, 1/1oz. Copper
C1, C4, C11	CHIP CAPACITOR 0.1uF, 0805, 100V
C2, C5, C6	CHIP CAPACITOR 27pF, 0805, ATC600F270
C3, C9	CHIP CAPACITOR 10uF, 2220, 50V, X7R
C7, C8	12pF, ATC 600F120 EDGE MNT
C10	CHIP CAPACITOR 12pF, ATC 600F120 EDGE MNT
C12	CHIP CAPACITOR 1uF, 1206, 100V
C3 (NOT SHOWN)	ELECTROLYTIC CAPACITOR, 4700uF / 50V
R1, R2, R3, R4	RESISTOR CHIP, 5R1, 0805
L1, L2	IND. FB, 120 OHM, 0805, 5A
L3	IND. SNS, 1508
GS (<6 PLACES)	GROUND SHIM, COPPER, TH=0.001"
CONN 1, CONN 2	SMA CONNECTOR, DS #2052-5636-02
INPUT PC BOARD CARRIER	2 INCH BRASS-3 (1")
OUTPUT PC BOARD CARRIER	2 INCH BRASS-3 (1")
TRANSISTOR CARRIER	2 INCH COPPER-26
TRANSISTOR CLAMP	NORYL CLAMP-14
ALUMINUM HEAT SINK	2 INCH HEATSINK-11
DC CONN 1	BANANA JACK, RED
DC CONN 2	BANANA JACK, BLACK
DC CONN 3	BANANA JACK, BLUE
NOTE	FIXTURE HARDWARE DRAWINGS AVAILABLE ON REQUEST

CIRCUIT DIMENSIONS



ELETRICAL SCHEMATIC



DEFINITIONS

Data Sheet Status	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
Maximum Ratings	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

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