

**S-Band Radar Transistor - GaN**

- GaN on SiC HEMT Technology
- $P_{OUT-PK} = 800W @ 100\mu s/5\%/50V$ ; ( $P_{AVG} = 40W$ )
- 2.7-2.9GHz Instantaneous Operating Frequency Range
- Internal Impedance Pre-matched Device – Single Ended
- Depletion Mode Device
- Negative Gate Voltage and Bias Sequencing Required
- Specified For Use Under Class AB Operation
- Metal Based Package Sealed With Ceramic-Epoxy Lid
- Gold Metallization System: Chip - Wire Bond - Package
- Package Size: W=1.620" (41.15mm), L=0.400" (10.16mm)
- 100% High Power RF Tested in Broadband RF Test Fixture

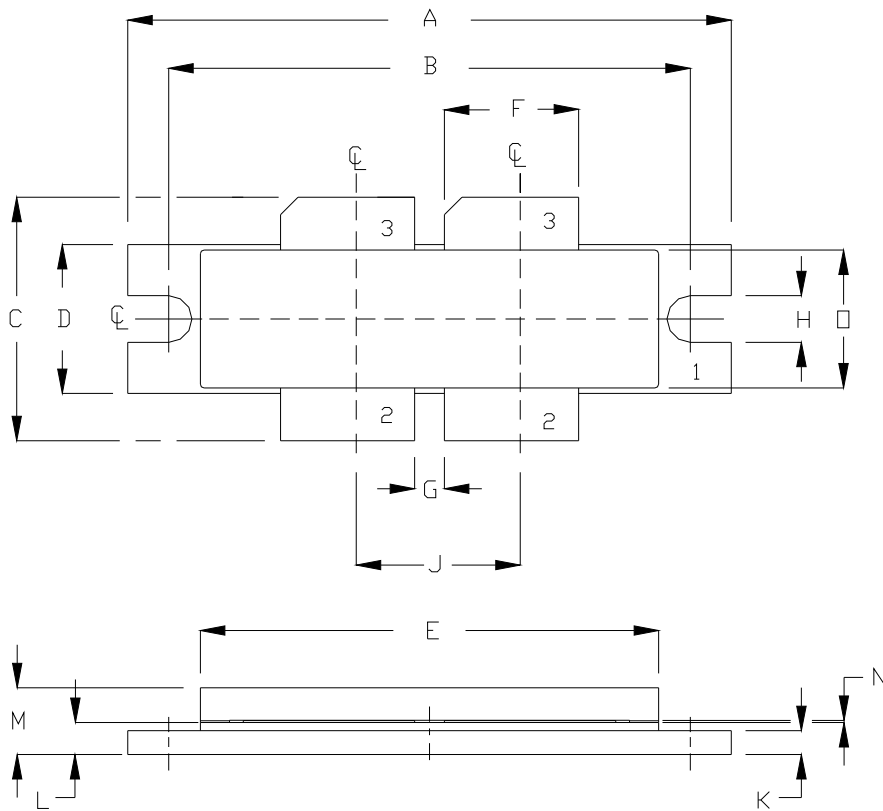


PARAMETER	SYM	MIN	TYP	MAX	UNITS	TEST CONDITIONS
<b>DC ELECTRICAL SPECIFICATIONS</b>						
Drain Leakage Current	$I_{D-OFF}$	--	--	6.0	mA	$V_{DS}=50V, V_{GS}=-6V, T_{F1}, S1$
Gate Threshold Voltage	$V_{GS-TH}$	--	-2.8	--	V	$V_{DS}=50V, I_D=100mA, T_{F1}, BD$
<b>RF ELECTRICAL SPECIFICATIONS</b>						
Input Return Loss	IRL	-18	-12	-7	dB	PIN1, V1, $I_{DQ1}$ , PW1, DF1, F1, F2, F3, $T_{F1}, S1$
Power Gain	GP	10.00	10.50	12.00	dB	PIN1, V1, $I_{DQ1}$ , PW1, DF1, F1, F2, F3, $T_{F1}, S1$
Power Output	PO	800	900	1265	W	PIN1, V1, $I_{DQ1}$ , PW1, DF1, F1, F2, F3, $T_{F1}, S1$
Drain Current	$I_D$	0	--	1000	A	PIN1, V1, $I_{DQ1}$ , PW1, DF1, F1, F2, F3, $T_{F1}, S1$
Drain Efficiency	$\eta_D$	55	60	75	%	PIN1, V1, $I_{DQ1}$ , PW1, DF1, F1, F2, F3, $T_{F1}, S1$
Pulse Amplitude Droop	D	-0.70	-0.40	+0.30	dB	PIN1, V1, $I_{DQ1}$ , PW1, DF1, F1, F2, F3, $T_{F1}, S1$
Delta Inter-pulse Insertion Phase	DIP	-30	--	+30	DEG	PIN1, V1, $I_{DQ1}$ , PW1, DF1, F1, F2, F3, $T_{F1}, S1$
Load Mismatch Stability	VSWR-S	3:1	3:1	--	--	PIN1, V1, $I_{DQ1}$ , PW1, DF1, F1, F2, F3, $T_{F1}, S1$
Load Mismatch Tolerance	LMT	3:1	3:1	--	--	PIN1, V1, $I_{DQ1}$ , PW1, DF1, F1, F2, F3, $T_{F1}, S1$
Output Power Flatness (10*Log Pout Max/Pin Max)	OPF	0	--	1.5	dB	PIN1, V1, $I_{DQ1}$ , PW1, DF1, F1, F2, F3, $T_{F1}, S1$
<b>DC &amp; RF TEST CONDITIONS</b>						
Input Power 1	PIN1	--	80	--	W	--
Drain Supply Voltage 1	V1	--	--	50.0	V	--
Quiescent Drain Current 1	$I_{DQ1}$	--	--	100	mA	--
Pulse Width 1	PW1	--	--	100	us	--
Duty Factor 1	DF1	--	--	5	%	--
Frequency 1	F1	--	2.7	--	GHz	--
Frequency 2	F2	--	2.8	--	GHz	--
Frequency 3	F3	--	2.9	--	GHz	--
Flange Temperature 1	$T_{F1}$	25	30	35	°C	--
Screening Level 1	S1	100	--	--	%	--

PARAMETER	SYM	MIN	MAX	UNITS	SCREEN	CONDITIONS
<b>MAXIMUM RATINGS</b>						
Drain-Source Voltage	$V_{DS}$	--	60	V	BD	$T_F = 25^\circ\text{C}$
Gate-Source Voltage	$V_{GS}$	-10	0	V	BD	$T_F = 25^\circ\text{C}$
Storage Temperature Range	$T_{STG}$	-55	+150	$^\circ\text{C}$	BD	--
Operating Junction Temperature	$T_J$	-55	+200	$^\circ\text{C}$	BD	--
<b>PROCESS SPECIFICATIONS</b>						
DC Wafer Probe	--	--	--	--	100%	Per Integra Spec
Wafer DC, RF Qualification	--	--	--	--	Q1	Per Integra Spec
Wire Bond Strength	--	--	--	--	LM	Per Integra Spec
Pre-cap Visual Inspection	--	--	--	--	100%	Per Integra Spec
Gross Leak Test – MIL-STD-750D	--	--	--	--	100%	Method 1071.6 C
<b>THERMAL RESISTANCE</b>						
Peak Thermal Resistance Per Rated RF Specification	$R_{TH(JC)}$	--	0.10	$^\circ\text{C/W}$	BD	$T_F = 25^\circ\text{C}$
<b>SCREENING LEVELS</b>						
Parameter Qualified By Design	BD	--	--	--	--	--
Parameter Qualified By 3 Pieces (min) Per Wafer	Q1	--	--	--	--	--
Parameter Qualified By Assembly Line Monitor	LM	--	--	--	--	--

RF TEST FIXTURE – BROADBAND		
▶ Broadband RF Test Fixture. Provides Device Impedance Matching to 50Ω Across the Rated Operating Frequency Range.		
▶ Electronic CAD Drawing File Available Upon Request. Includes Circuit Dimensions and Parts List.		
▶ Reference Design PCB: Rogers RO4350B-03011, DK=3.48.		
FREQUENCY (GHz)	$Z_{IF}(\Omega)$	$Z_{OF}(\Omega)$
2.7	$0.87 - j0.36$	$0.74 - j0.18$
2.8	$0.92 + j0.05$	$0.66 + j0.32$
2.9	$0.96 + j0.41$	$0.84 + j0.87$
Impedance Definition		

PACKAGE OUTLINE DRAWING



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.615	1.625	41.02	41.27
B	1.395	1.405	35.43	35.69
C	0.634	0.674	16.10	17.12
D	0.395	0.405	10.03	10.29
E	1.219	1.241	30.96	31.52
F	0.455	0.465	11.56	11.81
G	0.075	0.085	1.90	2.16
H	0.120	0.130	3.05	3.30
J	0.535	0.545	13.59	13.84
K	0.059	0.069	14.99	17.53
L	0.081	0.091	2.06	2.31
M	0.164	0.194	4.16	4.93
N	0.004	0.007	0.10	0.18
□	0.354	0.364	8.99	9.24

PIN SCHEDULE	
1	SOURCE
2	GATE
3	DRAIN

DEFINITIONS	
DATA SHEET STATUS	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
MAXIMUM RATINGS	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

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