

Part Number: **IGN5259CW50** (preliminary)

Integra

TECHNOLOGIES, INC.

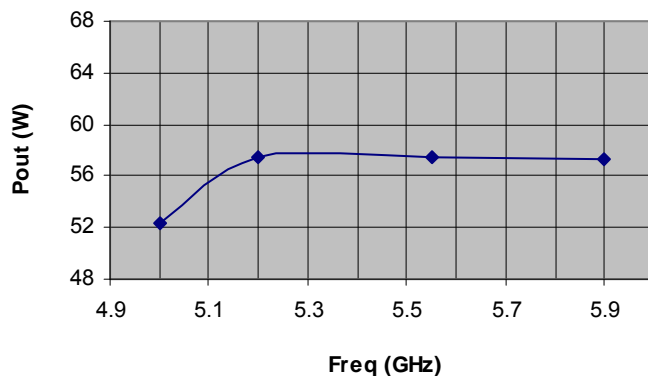
C-Band Power Transistor

IGN5259CW50 is an internally pre-matched, gallium nitride (GaN) high electron mobility transistor (HEMT). This part is designed for C-Band applications operating over the 5.2 – 5.9 GHz instantaneous frequency band. Under CW operating conditions it supplies a minimum of 50 watts of output power with 12dB gain typically. Specified operation is with Class AB bias. It operates with spectral purity into all phases of 3:1 output load VSWR. All devices are 100% screened for large signal RF parameters in a fixed tuned broadband matching circuit / test fixture. The use of external tuners is not allowed during screening. This device is rated for a CW output power level of 50W.

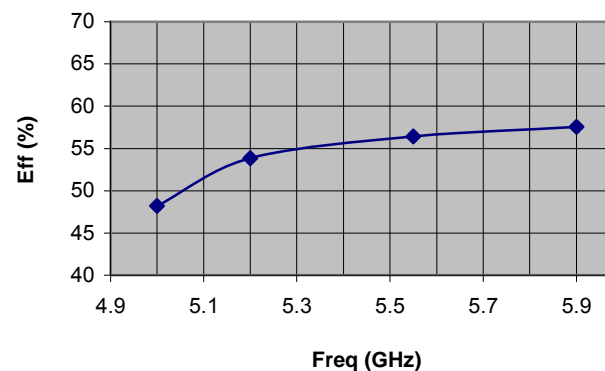


BROADBAND RF DATA

IGN525CW50
Pout vs Frequency
CW, Vdd = 24V, Idq = 80mA



IGN5259CW50
Efficiency
CW, Vdd = 24V, Idq = 80mA



GaN on Silicon Carbide FET

- High Power Gain
- Excellent Thermal Stability
- Gold Metal

Depletion Mode Device

- Negative Gate Voltage to Bias
- Bias Sequencing Required
- See App Note to Prevent Damage

Gold Metal System

- Complete Gold System
- Gold Bond Wires
- Gold Package Metal
- Maximum Reliability

Class AB

- Specified with AB bias

Internal Impedance Matching

- Ease of Use
- Input and Output
- Ultra Low Loss Design

Metal - Ceramic

- Metal Based
- Epoxy Seal

High Power RF Test / Fixture

- Broadband
- Matched to 50 Ω (ohms)
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning required

MAXIMUM RATINGS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Drain-Source Breakdown Voltage	V_{DS-BK}	80	--	V	--
BD	Drain-Source Voltage	V_{DS}	--	24	V	--
BD	Gate-Source Voltage	V_{GS}	-10	0	V	--
BD	Storage Temperature Range	T_{STG}	-55	+150	°C	--
BD	Operating Junction Temperature Range	T_J	-55	+200	°C	--
Note	Screen 'BD' = parameter qualified By Design.					

THERMAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	θ_{JC}	--	1.0	°C/W	$V_{DD}=V1, I_{DQ}=I_{DQ1}, CW, T_F=25\pm5^\circ C, P_{OUT}=50W$
Note	Screen 'BD' = parameter qualified By Design.					

PROCESSING SPECIFICATIONS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071.6, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					



DC ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
100%	Drain Leakage Current	I_{D-OFF}	--	10	--	mA	$V_{GS} = -8V, V_{DS} = 24V, T_F = 25\pm5^\circ C$
100%	Gate Threshold Voltage	V_{GS-TH}	--	-4.0	--	V	$V_{DS} = 24V, I_D = 80mA, T_F = 25\pm5^\circ C$

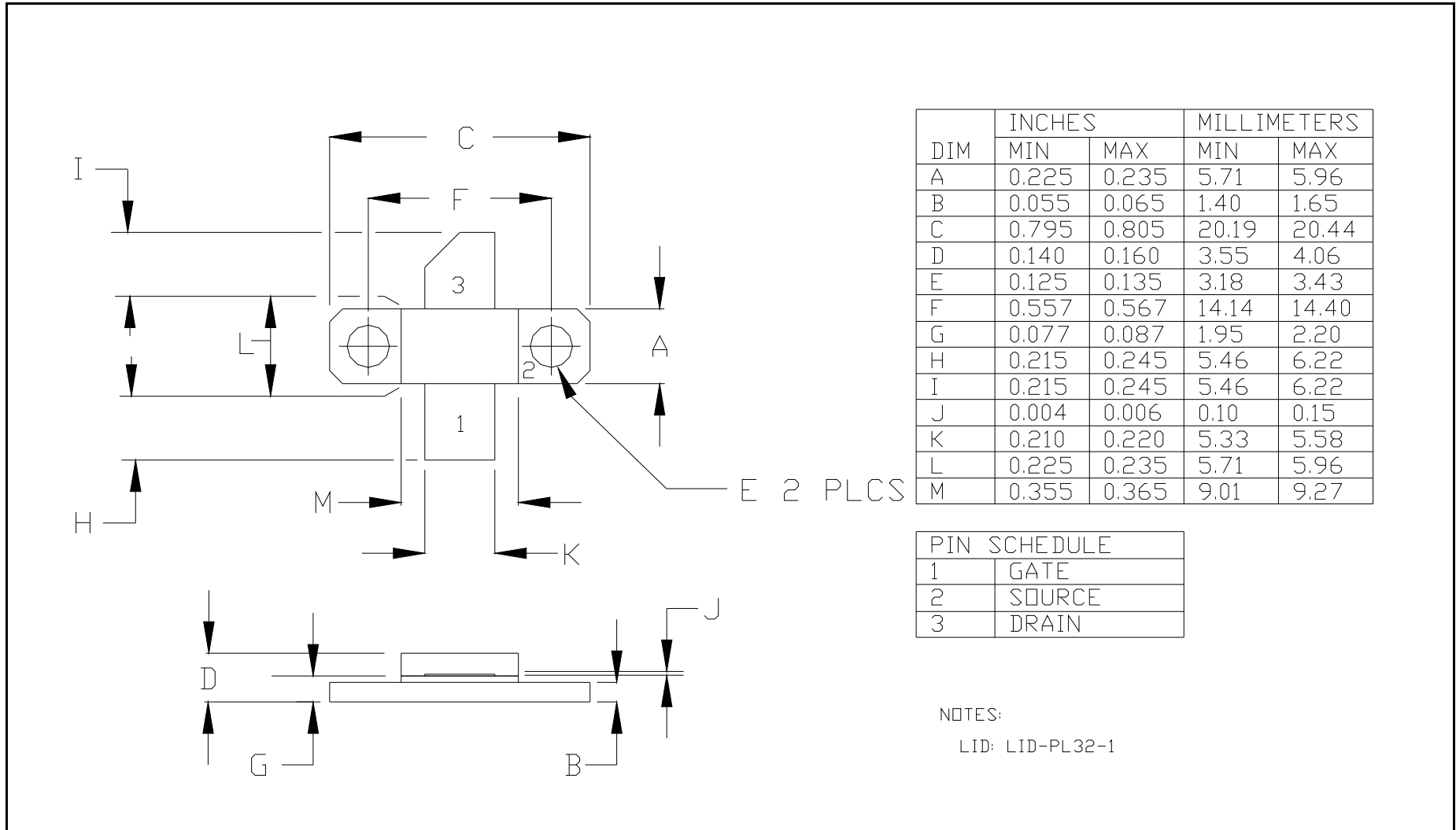
RF ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	IRL	-18	-8	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, CW, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Output Power	P_O	50	70	W	$V_{DD}=V1, I_{DQ}=I_{DQ1}, CW, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Drain Efficiency	N_d	50	65	%	$V_{DD}=V1, I_{DQ}=I_{DQ1}, CW, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Power Gain	Gp	11.5	14.0	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, CW, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	3:1 Load Mismatch Stability	VSWR-S	S	--	--	$V_{DD}=V1, I_{DQ}=I_{DQ1}, CW, T_F=T_{F1}, P_{OUT}=50W, F=F1, F2, F3.$ Rotate 3:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse. All non-harmonically related signals must be at least -65 dBc.
Note 1	$V1 = 24V; I_{DQ1} = 80mA$					
Note 2	Input Power Test Levels: $P_{IN1} = 3W$					
Note 3	Test Frequencies: $F1 = 5.20$ GHz, $F2 = 5.55$ GHz, $F3 = 5.90$ GHz.					
Note 4	$T_{F1} = 25 \pm 5^\circ C =$ Device flange temperature.					
Note 5	Screen 'BD' = parameter qualified By Design.					

RF TEST FIXTURE IMPEDANCE CHARACTERISTICS

Frequency (GHz)	$Z_{IF} (\Omega)$	$Z_{OF} (\Omega)$
5.20	4.0 – j13.0	6.1 – j8.1
5.55	3.2 – j10.1	5.7 – j6.0
5.90	3.1 – j8.1	6.8 – j3.9
Impedance Definition		

PACKAGE DIMENSIONAL OUTLINE DRAWING



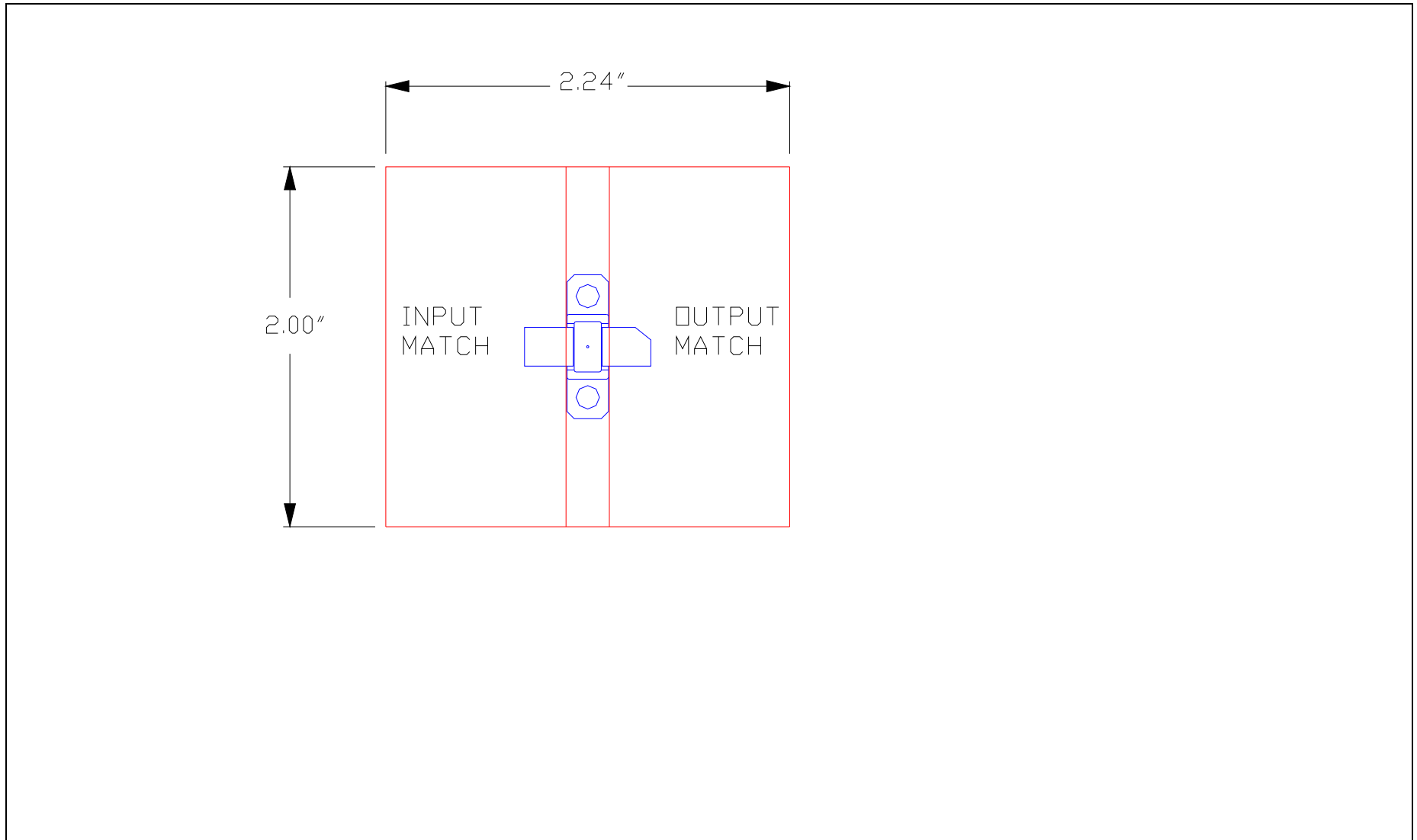
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.225	0.235	5.71	5.96
B	0.055	0.065	1.40	1.65
C	0.795	0.805	20.19	20.44
D	0.140	0.160	3.55	4.06
E	0.125	0.135	3.18	3.43
F	0.557	0.567	14.14	14.40
G	0.077	0.087	1.95	2.20
H	0.215	0.245	5.46	6.22
I	0.215	0.245	5.46	6.22
J	0.004	0.006	0.10	0.15
K	0.210	0.220	5.33	5.58
L	0.225	0.235	5.71	5.96
M	0.355	0.365	9.01	9.27

PIN SCHEDULE	
1	GATE
2	SOURCE
3	DRAIN

NOTES:

LID: LID-PL32-1

RF TEST FIXTURE



CONTACT FACTORY FOR RF TEST FIXTURE CAD DRAWING WITH CIRCUIT DIMENSIONS

DEFINITIONS

Data Sheet Status	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
Maximum Ratings	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

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