

# Part Number: **IGN5259M15 (Preliminary)**

# Integra

TECHNOLOGIES, INC.

## C-Band Radar Transistor

IGN5259M15 is an internally pre-matched, gallium nitride (GaN) high electron mobility transistor (HEMT). This part is designed for C-Band radar applications operating over the 5.2 – 5.9 GHz instantaneous frequency band. Under 300us / 10% pulse conditions it supplies a minimum of 15 watts of peak output power with 15dB gain typically. Specified operation is with Class AB bias. When appropriately rated, it is operable under a wide range of pulse widths and duty factors. It operates with spectral purity into all phases of 3:1 output load VSWR. All devices are 100% screened for large signal RF parameters in a fixed tuned broadband matching circuit / test fixture. The use of external tuners is not allowed during screening. This device is rated for a peak output power level of  $P_{PEAK} = 15W$  @ 10% duty factor. This corresponds to an average power  $P_{AVG} = 1.5W$ .



### GaN on Silicon Carbide FET

- High Power Gain
- Excellent thermal stability

### Depletion Mode Device

- Negative Gate Voltage to Bias
- Bias Sequencing Required
- See App Note to Prevent Damage

### Gold Metal System

- Complete Gold System
- Gold Bond Wires
- Gold Package Metal
- Maximum Reliability

### Class AB

- Specified with AB bias

### Internal Impedance Matching

- Ease of Use
- Input and Output

### Metal - Ceramic Package

- Metal Based
- Epoxy Seal

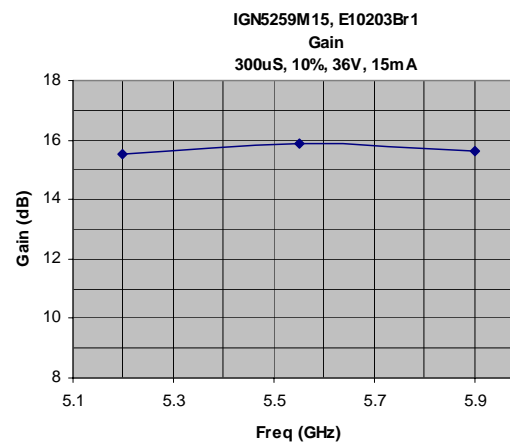
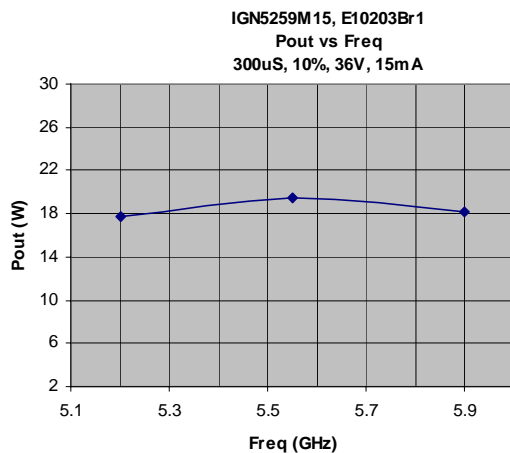
### High Power 50Ω RF Test / Fixture

- Broadband
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning required

### Patent Issued

- US 8,299,857 B2

## SAMPLE DEVELOPMENT DATA



**MAXIMUM RATINGS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Drain-Source Voltage	$V_{DS}$	--	40	V	--
BD	Gate-Source Voltage	$V_{GS}$	-12	0	V	--
BD	Storage Temperature Range	$T_{STG}$	-55	+150	°C	--
BD	Operating Junction Temperature Range	$T_J$	-55	+200	°C	--
BD	CW Operation	--	--	--	--	Not rated for CW operation
Note	Screen 'BD' = parameter qualified By Design.					

**THERMAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	1.41	°C/W	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{OUT}=15W, N_D=45\%$
Note	Screen 'BD' = parameter qualified By Design.					

**PROCESSING SPECIFICATIONS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071.6, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					



**DC ELECTRICAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
100%	Drain Leakage	$I_{D-off}$	--	0.2	--	mA	$V_{DS} = 80V, V_{GS} = -8V, T_F = 25\pm5^\circ C$
100%	Threshold Voltage	$V_{GS-TH}$	--	-3.5	--	V	$V_{DS} = 36V, I_D = 0.100A, T_F = 25\pm5^\circ C$

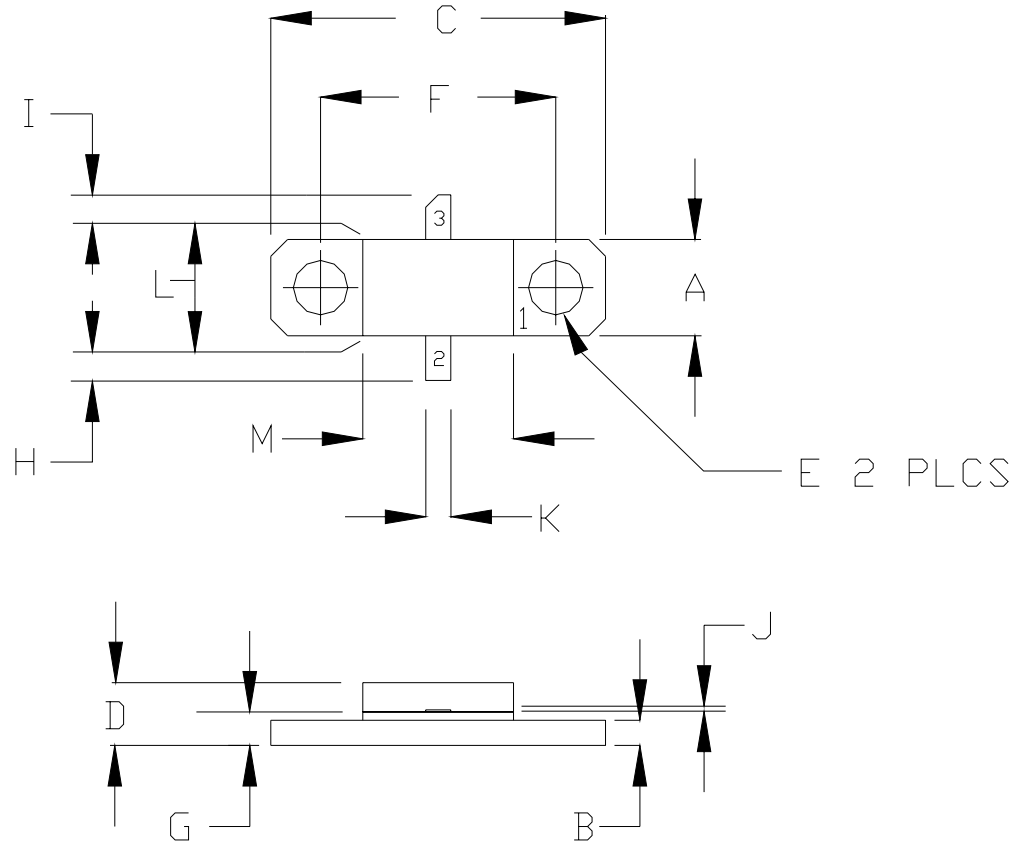
**RF ELECTRICAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	RL	-18	-7	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Output Power	$P_O$	15	25	W	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Drain Current – Peak	$I_D$	0.85	1.00	A	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Pulse Amplitude Droop	Droop	0.5	-0.5	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Power Gain	$G_p$	14.8	17.0	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	3:1 Load Mismatch Stability	VSWR-S	S	--	--	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{out}=40W, F=F1, F2, F3.$ Rotate 3:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse. All non-harmonically related signals must be at least -65 dBc.
Note 1	$V1 = 36V; I_{DQ1} = 15mA; PW1 = 300us; DF1 = 10%$					
Note 2	Input Power Test Levels: $P_{IN1} = 0.5W$					
Note 3	Test Frequencies: $F1 = 5.20\text{ GHz}, F2 = 5.55\text{ GHz}, F3 = 5.90\text{ GHz}.$					
Note 4	$T_{F1} = 25\pm5^\circ\text{C}$ = Device flange temperature.					
Note 5	Screen 'BD' = parameter qualified By Design.					

**RF TEST FIXTURE IMPEDANCE CHARACTERISTICS**

Frequency (GHz)	$Z_{IF} (\Omega)$	$Z_{OF} (\Omega)$
5.20	$7.2 - j17$	$9.4 - j3.6$
5.55	$12.1 - j13$	$10.8 - j1.5$
5.90	$9.4 - j9$	$9.2 + j0.6$
Impedance Definition		

**PACKAGE DIMENSIONAL OUTLINE DRAWING**



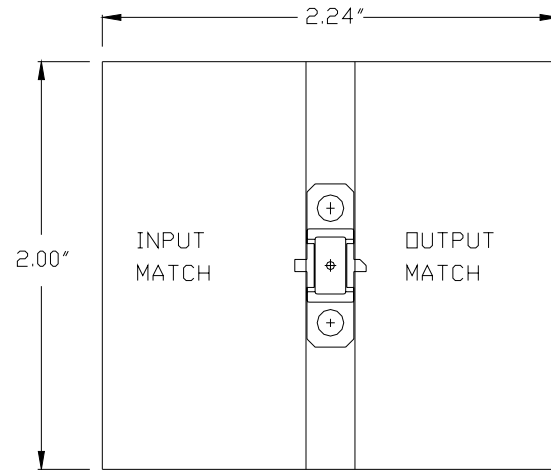
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.225	0.235	5.71	5.96
B	0.055	0.065	1.40	1.65
C	0.795	0.805	20.19	20.44
D	0.140	0.160	3.55	4.06
E	0.125	0.135	3.18	3.43
F	0.557	0.567	14.14	14.40
G	0.077	0.087	1.95	2.20
H	0.093	0.107	2.36	2.72
I	0.093	0.107	2.36	2.72
J	0.004	0.006	0.10	0.15
K	0.055	0.065	1.40	1.65
L	0.225	0.235	5.71	5.96
M	0.355	0.365	9.01	9.27

PIN SCHEDULE	
1	SOURCE
2	GATE
3	DRAIN

NOTES:

LID: LID-PL32-1

**RF TEST FIXTURE**



CONTACT FACTORY FOR DETAILED RF TEST FIXTURE CAD DRAWING

**DEFINITIONS**

<b>Data Sheet Status</b>	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
<b>Maximum Ratings</b>	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

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