

Part Number: **ILD1011M1100HV (Preliminary)**

Integra

TECHNOLOGIES, INC.

Avionics Band RF Power LDMOS FET

The high power transistor part number ILD1011M1100HV is designed for Avionics systems operating at 1030 MHz. Operating at 100 μ s, 5% pulse conditions this LDMOS FET device supplies a minimum of 1100 watts of power at 1030 MHz. All devices are 100% screened for large signal RF parameters.

Silicon LDMOS FET

- High Power Gain
- Superior thermal stability

Class AB Operation

- Gate biased to $I_{DQ} = 60$ mA

Configuration

- Common Source

Gold Metal

- Maximum Reliability

Package

- Thermally enhanced
- Pb-free and RoHS-compliant

Epoxy Sealed Lid

- Gross Leak Qualified

RF Test Fixture

- Broadband
- Matched to 50 ohms
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning required

PRELIMINARY DATA

PRELIMINARY DATA

PRELIMINARY DATA

Lot/SN	Freq (MHz)	P _i (W)	I _D (A)	RL (dB)	P _o (W)	Nd' (%)	G (dB)	VSWR	
								3:1	20:1
50028376-4	1030	20	39.28	15.5	1127	57.4	17.5	S	P

Pulse format = 100 μ s, 5% $I_{DQ} = 60$ mA, $V_d = 50$ V

MAXIMUM RATINGS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Drain-Source Voltage	V_{DS}	--	92	V	--
BD	Gate-Source Voltage	V_{GS}	--	20	V	--
BD	Storage Temperature Range	T_{STG}	-55	+200	°C	--
BD	Operating Junction Temperature Range	T_J	-55	+200	°C	--
Note	Screen 'BD' = parameter qualified By Design.					

THERMAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	TBD	°C/W	$V_D=50V, I_{DQ}=60mA, T_F=25\pm5^\circ C, P_{OUT}=1100W$
Note	Screen 'BD' = parameter qualified By Design.					

PROCESSING SPECIFICATIONS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

DC ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Drain-Source Breakdown Voltage	BV_{DSS}	92	--	V	$I_D = 70mA, V_{GS} = 0V, T_F = 25\pm5^\circ C$
100%	Drain Leakage Current	I_{DSS}	--	48	μA	$V_{DS} = 50V, V_{GS} = 0V, T_F = 25\pm5^\circ C$
100%	Gate Threshold Voltage	V_{GSTH2}	2.75	5.25	V	$I_D = 100mA, T_F = 25\pm5^\circ C, V_{DS} = 5V$
100%	Gate Leakage Current	I_{GSS}	--	1	μA	$V_{GS} = 5V, V_{DS} = 0V, T_F = 25\pm5^\circ C$

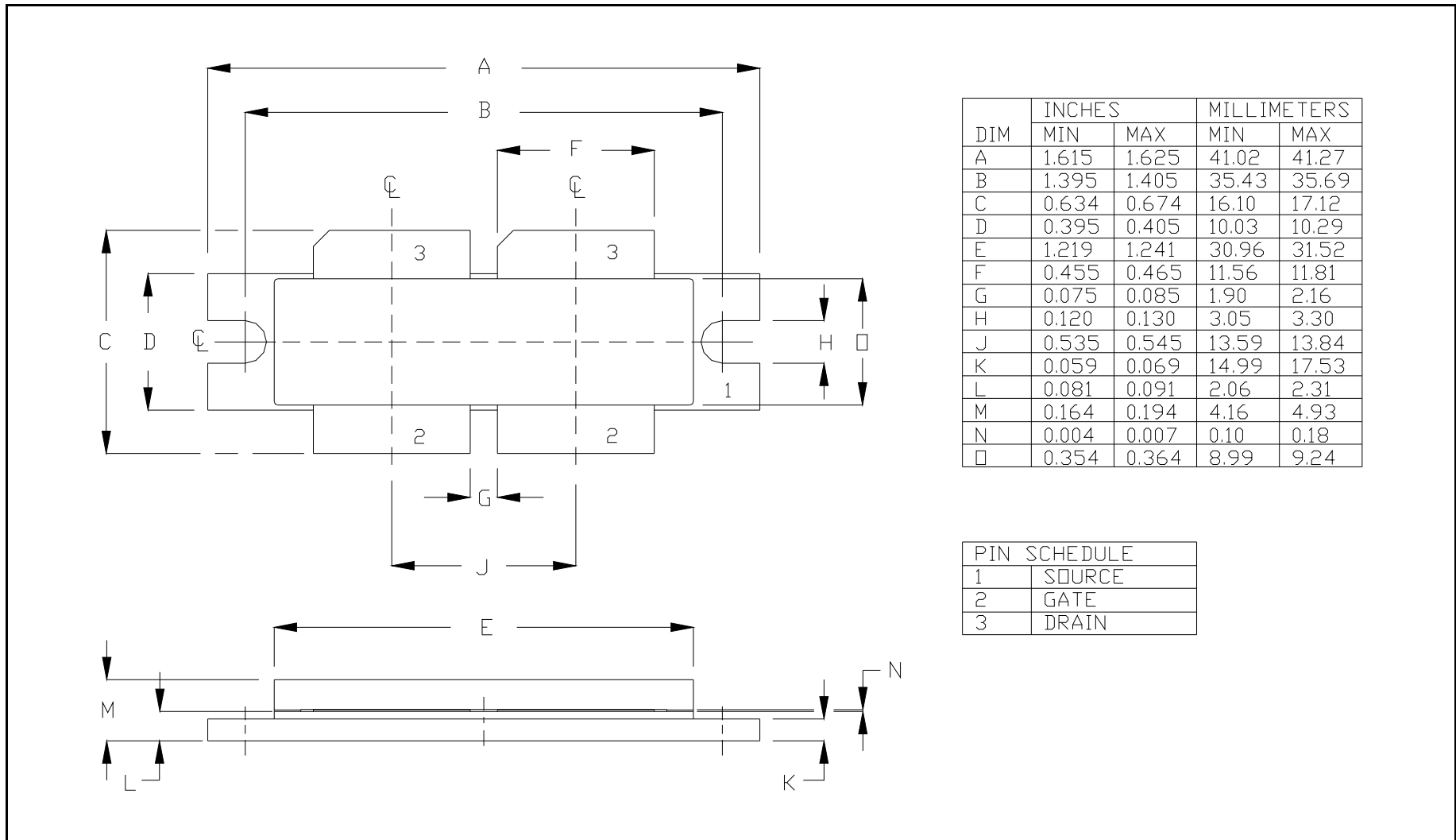
RF ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	IRL	10	--	dB	$V_{DD}=50V$, $P_{in}=20W$, Pulse=100 μ s, 5%, $T_F=25\pm 5^\circ C$, $F=F1$, $I_{DQ}=60mA$.
BD	Maximum Overdrive	$P_{IN(MAX)}$	--	27	W	$V_{DD}=50V$, Pulse=100 μ s, 5%, $T_F=25\pm 5^\circ C$, $F=F1$, $I_{DQ}=60mA$.
100%	Power Gain	G_P	17.4	18.9	dB	$V_{DD}=50V$, $P_{in}=20W$, Pulse=100 μ s, 5%, $T_F=25\pm 5^\circ C$, $F=F1$, $I_{DQ}=60mA$.
100%	Output Power	P_{out}	1100	1552	W	$V_{DD}=50V$, $P_{in}=20W$, Pulse=100 μ s, 5%, $T_F=25\pm 5^\circ C$, $F=F1$, $I_{DQ}=60mA$.
100%	Drain Efficiency	η'_d	50	75	%	$V_{DD}=50V$, $P_{in}=20W$, Pulse=100 μ s, 5%, $T_F=25\pm 5^\circ C$, $F=F1$, $I_{DQ}=60mA$.
100%	Pulse Amplitude Droop	D	-0.5	+0.5	dB	$V_{DD}=50V$, $P_{in}=20W$, Pulse=100 μ s, 5%, $T_F=25\pm 5^\circ C$, $F=F1$, $I_{DQ}=60mA$.
100%	Stability into 3:1 VSWR	VSWR-S		3:1	--	$V_{DD}=50V$, $P_{in}=20W$, Pulse=100 μ s, 5%, $T_F=25\pm 5^\circ C$, $F=F1$, $I_{DQ}=60mA$. Rotate 3:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse.
BD	Load Mismatch Tolerance	LMT		20:1	--	$V_{DD}=50V$, $P_{in}=20W$, Pulse=100 μ s, 5%, $T_F=25\pm 5^\circ C$, $F=F1$, $I_{DQ}=60mA$. Rotate 20:1 output VSWR through 360° phase. Survival.
BD	Pulse Risetime	RT		60	ns	$V_{DD}=50V$, $P_{in}=20W$, Pulse=100 μ s, 5%, $T_F=25\pm 5^\circ C$, $F=F1$, $I_{DQ}=60mA$. Measure between 10% and 90% detected power points.
Note 1	F1 = 1030MHz.					
Note 2	Pulse format = 100 μ s, 5%					
Note 3	T_F = Device flange temperature.					
Note 4	Screen 'BD' = parameter qualified By Design.					

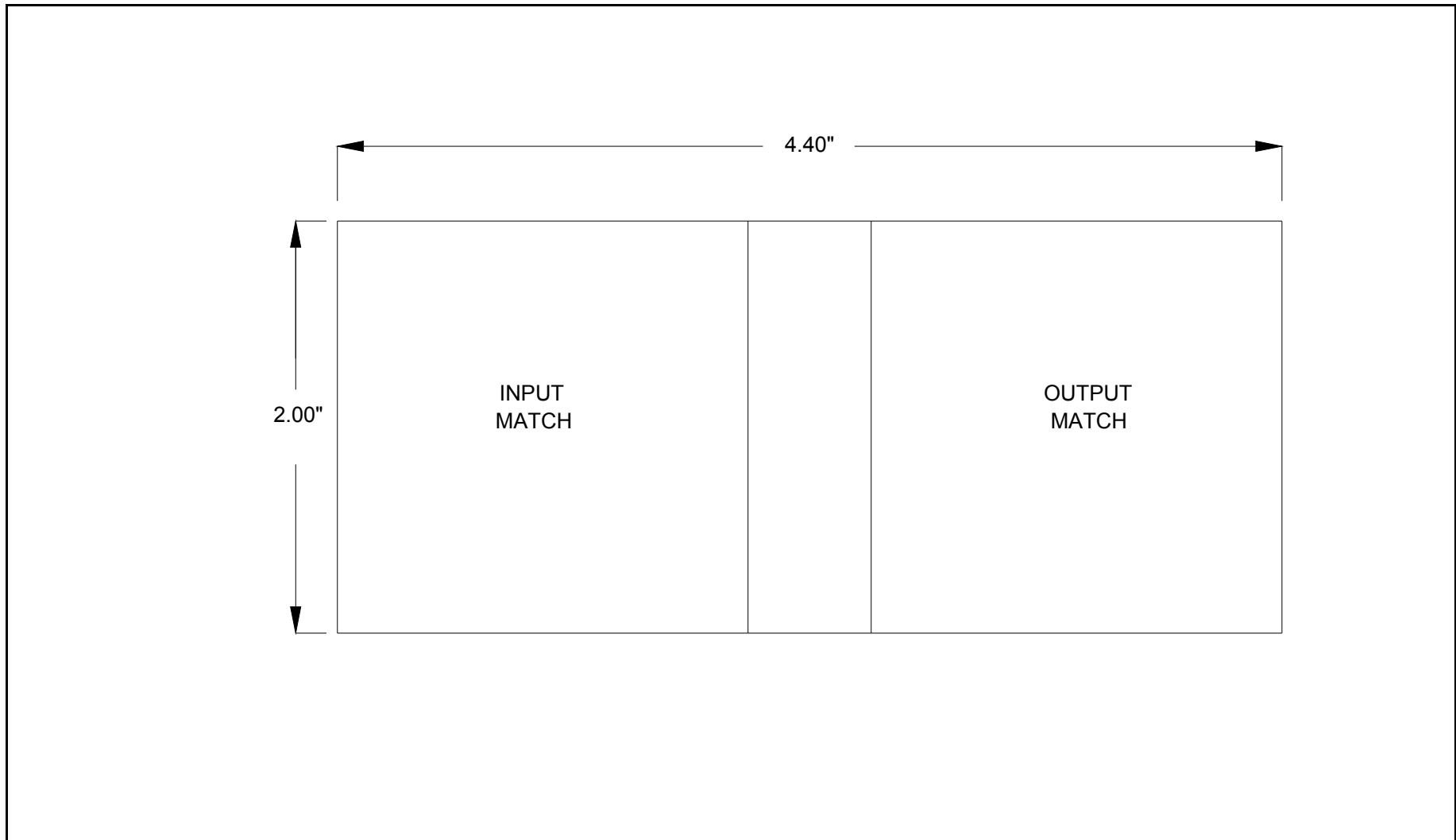
RF TEST FIXTURE IMPEDANCE CHARACTERISTICS

Frequency (MHz)	Z_{IF} (Ω)	Z_{OF} (Ω)
1030	$0.81 + j1.14$	$0.87 + j1.88$
Impedance Definition		

PACKAGE DIMENSIONAL OUTLINE DRAWING



RF TEST FIXTURE



CONTACT FACTORY FOR RF TEST FIXTURE CAD DRAWING WITH CIRCUIT DIMENSIONS

DEFINITIONS

Data Sheet Status	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
Maximum Ratings	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only. Operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

DISCLAIMER

Integra Technologies Inc. reserves the right to make changes without further notice to any products herein. Integra Technologies Inc. makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Integra Technologies Inc. assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. Integra Technologies Inc. products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Integra Technologies Inc. customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Integra Technologies Inc. for any damages resulting from such improper use or sale.