Part Number: ILD1011M15

Integra
TECHNOLOGIES, INC.

Avionics Band RF Power LDMOS FET

The high power transistor part number ILD1011M15 is designed for Avionics systems operating at 1030-1090 MHz. This LDMOS FET device under 50us, 2% pulse format supplies a minimum of 15 watt of peak pulse power. All devices are 100% screened for large signal parameters.

Silicon LDMOS FET
- High Power Gain
- Superior thermal stability
- Gold Metal

Class AB Operation
- Gate biased to I_{DQ}=10mA

Configuration
- Common Source

Gold Metal
- Maximum Reliability

BeO - Free Package
- Metal Based
- Epoxy Seal

Epoxy Sealed Lid
- Gross Leak Qualified

RF Test Fixture
- Broadband
- Matched to 50Ω
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning Allowed

TYPICAL DATA *TYPICAL DATA* *TYPICAL DATA* *TYPICAL DATA*

Freq (MHz)	PIN (W)	RL (dB)	POUT (W)	GP (dB)	Id (A)	nd (%)	VSWR-S 3:1 (P:F)
1030	0.75	-13.0	20.5	14.4	2.15	44.4	P
1090	0.75	-18.0	19.36	14.1	2.05	44.5	P

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MAXIMUM RATINGS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Drain-Source Voltage	V_{DS}	--	65	V	--
BD	Gate-Source Voltage	V_{GS}	-0.5	12	V	--
BD	Storage Temperature Range	T_{STG}	-55	+150	°C	--
BD	Operating Junction Temperature Range	T_J	-55	+200	°C	--
Note	Screen 'BD' = parameter qualified By Design.					

THERMAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	0.34	°C/W	V_{DS} =28V, I_{DQ}=10mA, T_F = 25±5°C, P_{IN} =0.75W
Note	Screen 'BD' = parameter qualified By Design.					

PROCESSING SPECIFICATIONS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

DC ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Drain-Source Breakdown Voltage	BV_{DSS}	65	--	V	I_{DS} =10mA, V_{GS} =0V, T_F =25±5°C.
100%	Drain Leakage Current	I_{DSS}	--	1.0	uA	V_{DS} =28V, V_{GS} =0V, T_F =25±5°C.
100%	Operating Gate Voltage	V_{GS}	2.5	4.0	V	V_{DS} =5V, T_F =25±5°C, I_{DS}=100mA.
100%	Gate Leakage Current	I_{GSS}	--	1.0	uA	V_{GS} =5V, V_{DS} =0V, T_F =25±5°C.

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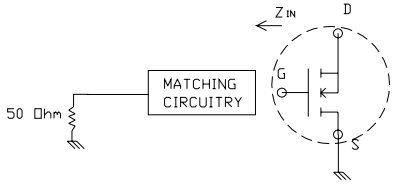
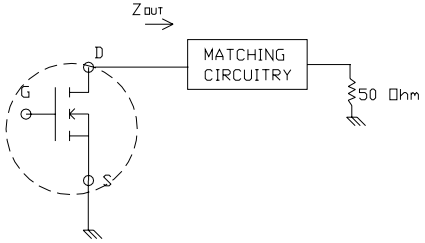
RF ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	RL	-18	-10	dB	V_{DS}=28V, Pin=0.75W, Pulse=PW1 @ F1, F2, T_F=25±5°C, I_{DQ}=10mA.
100%	Drain Efficiency	Nd	40	80	W	V_{DS}=28V, Pin=0.75W, Pulse=PW1 @ F1, F2, T_F=25±5°C, I_{DQ}=10mA.
100%	Power Gain	Gp	13	20	dB	V_{DS}=28V, Pin=0.75W, Pulse=PW1 @ F1, F2, T_F=25±5°C, I_{DQ}=10mA.
100%	Output Power	Pout	15	75	W	V_{DS}=28V, Pin=0.75W, Pulse=PW1 @ F1, F2, T_F=25±5°C, I_{DQ}=10mA.
100%	Stability into 3:1 VSWR	VSWR-S	--	3:1	--	V_{DS}=28V, Pin=0.75W, Pulse=PW1 @ F1, F2, T_F=25±5°C, I_{DQ}=10mA Rotate 3:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse.
BD	Load Mismatch Tolerance	VSWR-LMT	--	3:1	--	V_{DS}=28V, Pin=0.75W, Pulse=PW1 @ F1, F2, T_F=25±5°C, I_{DQ}=10mA, Rotate 20:1 output VSWR through 360° phase.
Note 1	F1=1030 MHz, F2=1090 MHz.					
Note 2	Pulse format: PW1= 50us, 2%					
Note 3	T_F = Device flange temperature.					
Note 4	Screen 'BD' = parameter qualified By Design.					

RF TEST FIXTURE IMPEDANCE CHARACTERISTICS

Frequency (MHz)	Z_{IF} (Ω)	Z_{OF} (Ω)
1030	2.1 –j1.9	15.9 –j11.7
1090	1.9 –j1.9	14.3 –j10.9
Impedance Definition		

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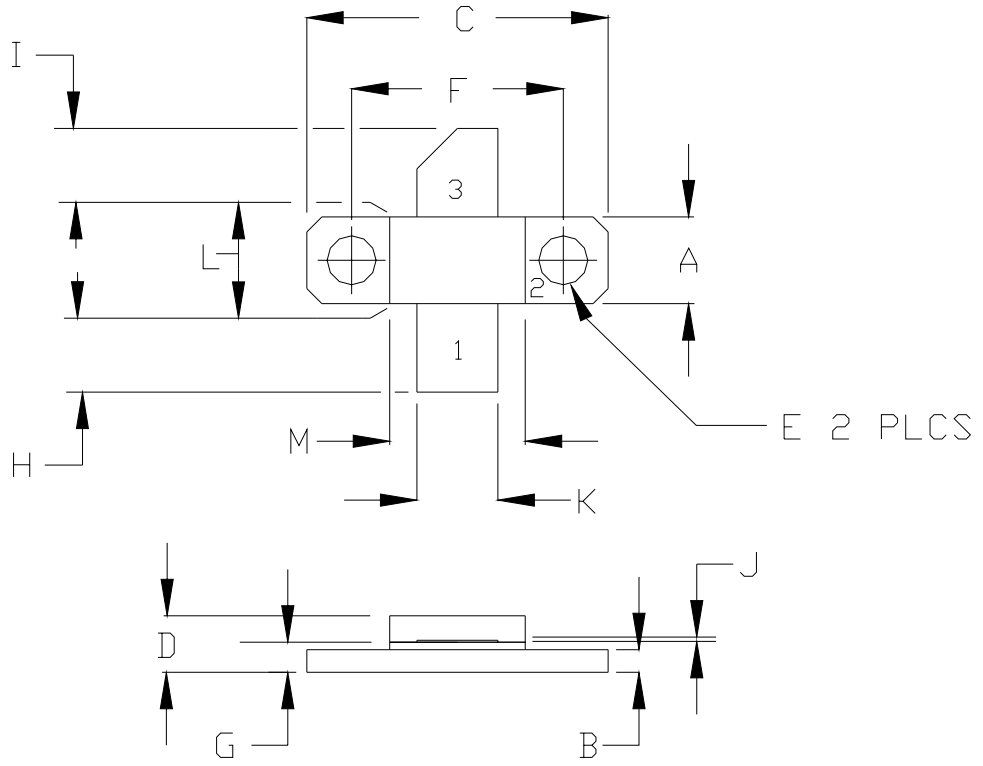
PACKAGE DIMENSIONAL OUTLINE DRAWING



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.225	0.235	5.71	5.96
B	0.055	0.065	1.40	1.65
C	0.795	0.805	20.19	20.44
D	0.140	0.160	3.55	4.06
E	0.125	0.135	3.18	3.43
F	0.557	0.567	14.14	14.40
G	0.077	0.087	1.95	2.20
H	0.215	0.245	5.46	6.22
I	0.215	0.245	5.46	6.22
J	0.004	0.006	0.10	0.15
K	0.210	0.220	5.33	5.58
L	0.225	0.235	5.71	5.96
M	0.355	0.365	9.01	9.27

PIN	SCHEDULE
1	GATE
2	SOURCE
3	DRAIN

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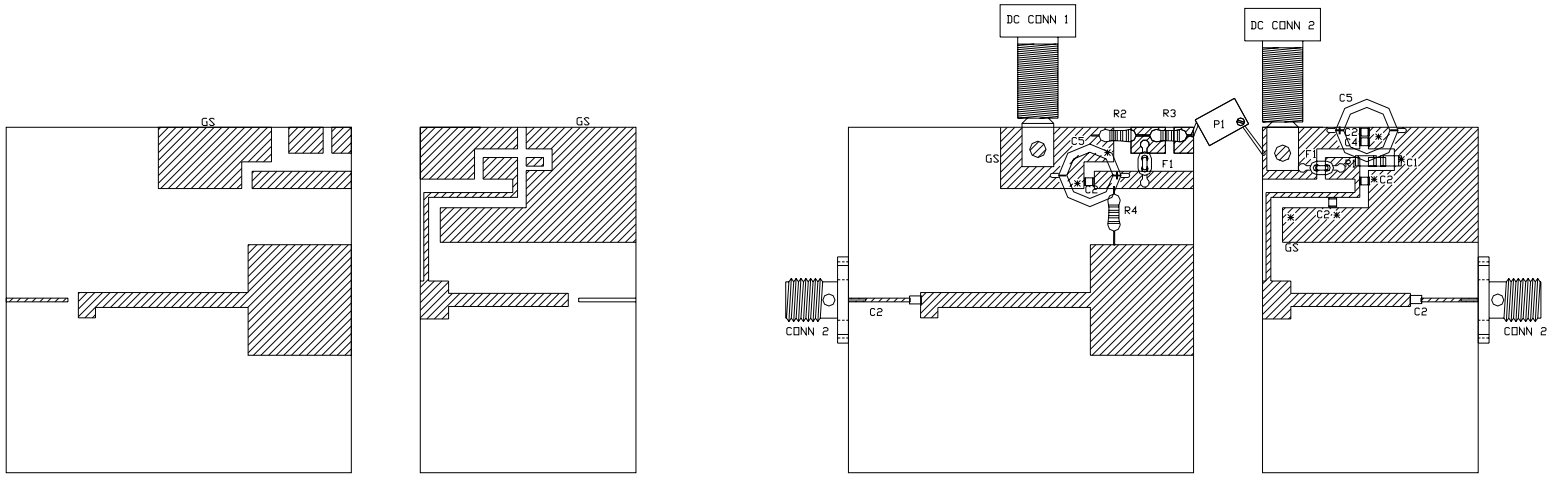
RF TEST FIXTURE



COMPONENT	DESCRIPTION
DUT	TRANSISTOR #IILD1011M15 MOUNT HARD TO THE RIGHT
PC BOARD	ROGERS #RT6010.2LM 2E/2E .025"
C1	SNUB CAPACITOR 0.1uF
C2	CHIP CAPACITOR ATC100A 100pF
C3 (NOT SHOWN)	ELECTROLYTIC CAPACITOR 4700uF / 50V
C4	CHIP CAPACITOR ATC100A 4.7uF
C5	ELECTROLYTIC CAPACITOR 68uF
R1	SNUB RESISTOR 6.81 Ohms
R2	RESISTOR 12 K Ohms
R3	RESISTOR 68 K Ohms
R4	RESISTOR 1 M Ohms
F1	BIAS WITH FERRITE BEAD
P1	POTENTIOMETER 100K Ohms
GS (7 PLACES)	GROUND SHIM, COPPER, TH=0.001"
CONN 1, CONN 2	SMA CONNECTOR, DS #2052-5636-02
INPUT PC BOARD CARRIER	2 INCH BRASS-07 (2")
OUTPUT PC BOARD CARRIER	2 INCH BRASS-04 (1.25")
TRANSISTOR CARRIER	2 INCH COPPER-05 (PL32)
TRANSISTOR CLAMP	NORYL CLAMP-07
ALUMINUM HEAT SINK	2 INCH HEATSINK-09
DC CONN 1	BANANA JACK, BLACK
DC CONN 2	BANANA JACK, RED
NOTE	FIXTURE HARDWARE DRAWINGS AVAILABLE ON REQUEST

ASSEMBLY AND PARTS LIST

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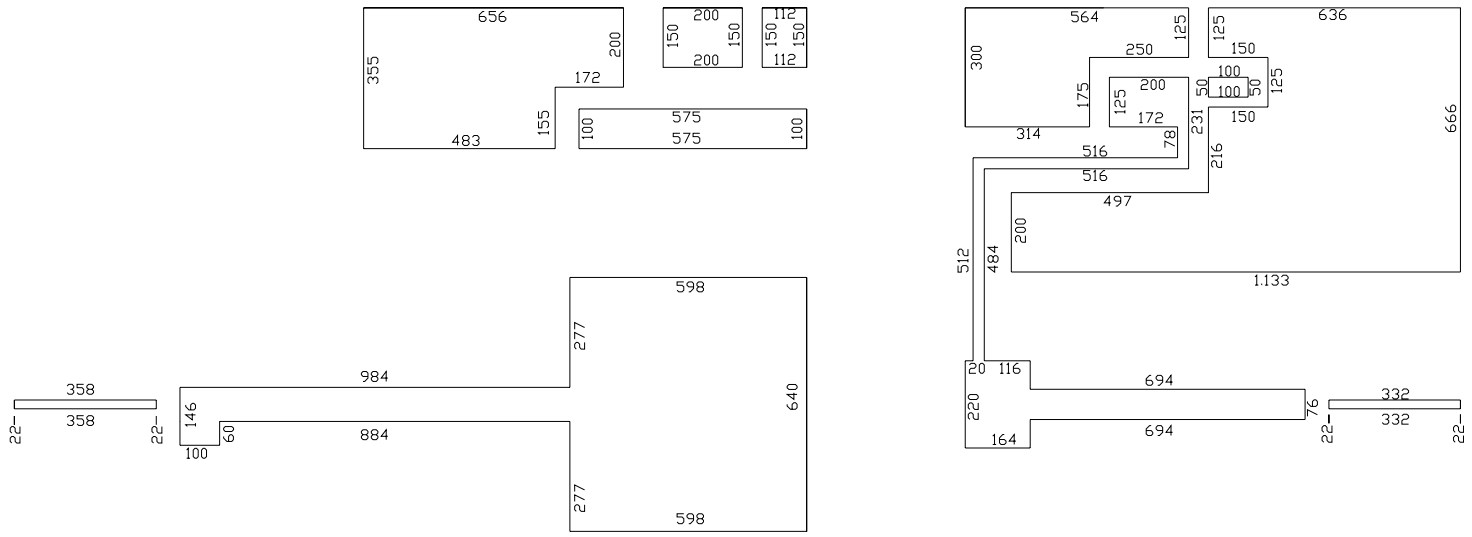

CIRCUIT DIMENSIONS

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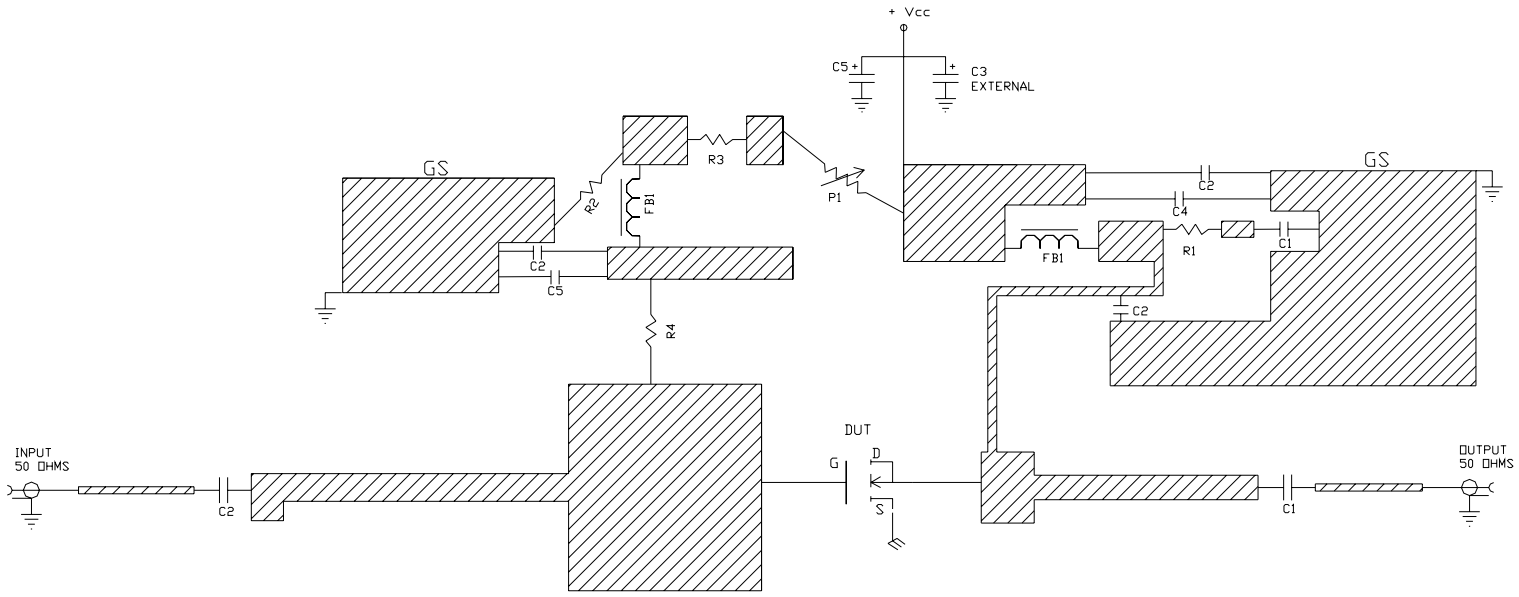

ELECTRICAL SCHEMATIC

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DEFINITIONS

Data Sheet Status	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.

Maximum Ratings
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only. Operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.

DISCLAIMER

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