

**Avionics Band RF Power LDMOS FET**

The high power transistor part number ILD1011M250 is designed for Avionics systems operating at 1030-1090 MHz. Operating at 50µs, 2% pulse conditions this LDMOS FET device supplies a minimum of 250 watts of power at 1030/1090 MHz. All devices are 100% screened for large signal RF parameters.



**Silicon LDMOS FET**

- High Power Gain
- Superior thermal stability

**Class AB Operation**

- Gate biased to  $I_{DQ} = 20 \text{ mA}$

**Configuration**

- Common Source

**Gold Metal**

- Maximum Reliability

**Package**

- Thermally enhanced
- Pb-free and RoHS-compliant

**Epoxy Sealed Lid**

- Gross Leak Qualified

**RF Test Fixture**

- Broadband
- Matched to 50 ohms
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning required

*TYPICAL DATA    TYPICAL DATA    TYPICAL DATA    TYPICAL DATA*

Devices	Feq (MHz)	V <sub>DD</sub> (V)	P <sub>IN</sub> (W)	P <sub>OUT</sub> (W)	Gain (dB)	I <sub>pk</sub> (A)	nd (%)	Droop (dB)	VSWR	
									1.5:1	20:1
50030075-2	1090	40	11	280	14.06	12.55	56	0	S	P

Pulse format = 50µs, 2%, I<sub>DQ</sub> = 30mA

n<sub>d</sub> = Drain efficiency (including bias current)

**MAXIMUM RATINGS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Drain-Source Voltage	$V_{DS}$	--	70	V	--
BD	Gate-Source Voltage	$V_{GS}$	--	20	V	--
BD	Storage Temperature Range	$T_{STG}$	-55	+150	°C	--
BD	Operating Junction Temperature Range	$T_J$	-55	+200	°C	--
Note	Screen 'BD' = parameter qualified By Design.					

**THERMAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	0.033	°C/W	$V_D=40V, I_{DQ}=20mA, T_F=25\pm 5^\circ C, P_{OUT}=250W$
Note	Screen 'BD' = parameter qualified By Design.					

**PROCESSING SPECIFICATIONS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

**DC ELECTRICAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Drain-Source Breakdown Voltage	$BV_{DSS}$	100	--	V	$I_D=20mA, V_{GS}=0V, T_F=25\pm 5^\circ C$
100%	Drain Leakage Current	$I_{DSS}$	--	100	$\mu A$	$V_{DS}=40V, V_{GS}=0V, T_F=25\pm 5^\circ C$
100%	Gate Threshold Voltage	$V_{GS}$	2.5	5.0	V	$I_D=100mA, V_{DS}=5V, T_F=25\pm 5^\circ C$
100%	Gate Leakage Current	$I_{gss}$	--	1	$\mu A$	$V_{GS}=10V, V_{DS}=0V, T_F=25\pm 5^\circ C$

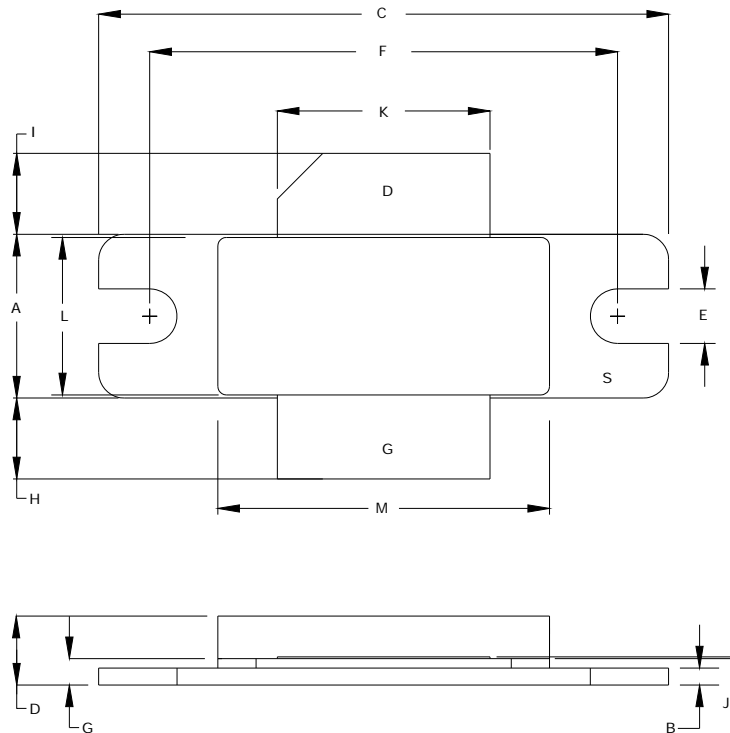
**RF ELECTRICAL CHARACTERISTICS**

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	IRL	10		dB	$V_{DD}=40V$ , $P_{IN}=11W$ , Pulse=50 $\mu$ s, 2%, $T_F=25\pm 5^\circ C$ , F=F1, $I_{DQ}=20mA$ .
100%	Output Power	$P_{OUT}$	250		W	$V_{DD}=40V$ , $P_{IN}=11W$ , Pulse=50 $\mu$ s, 2%, $T_F=25\pm 5^\circ C$ , F=F1, $I_{DQ}=20mA$ .
100%	Drain Efficiency ( $P_o/I_D/V_{DD}$ )	$N_d$	42		%	$V_{DD}=40V$ , $P_{IN}=11W$ , Pulse=50 $\mu$ s, 2%, $T_F=25\pm 5^\circ C$ , F=F1, $I_{DQ}=20mA$ .
100%	Pulse Amplitude Droop	D	-0.30	+0.20	dB	$V_{DD}=40V$ , $P_{IN}=11W$ , Pulse=50 $\mu$ s, 2%, $T_F=25\pm 5^\circ C$ , F=F1, $I_{DQ}=20mA$ .
100%	Stability into 1.5:1 VSWR	VSWR-S			--	$V_{DD}=40V$ , $P_{IN}=11W$ , Pulse=50 $\mu$ s, 2%, $T_F=25\pm 5^\circ C$ , F=F1, $I_{DQ}=20mA$ . Rotate 1.5:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse.
BD	Load Mismatch Tolerance	LMT		20:1	--	$V_{DD}=40V$ , $P_{OUT}=250W$ , Pulse=50 $\mu$ s, 2%, $T_F=25\pm 5^\circ C$ , F=F1, $I_{DQ}=20mA$ . Rotate 20:1 output VSWR through 360° phase. Survival.
BD	Pulse Risetime	RT		60	ns	$V_{DD}=40V$ , $P_{IN}=11W$ , Pulse=50 $\mu$ s, 2%, $T_F=25\pm 5^\circ C$ , F=F1, $I_{DQ}=20mA$ . Measure between 10% and 90% detected power points.
Note 1	F1 = 1090 MHz.					
Note 2	Pulse format = 50 $\mu$ s, 2%					
Note 3	$T_F$ = Device flange temperature.					
Note 4	Screen 'BD' = parameter qualified By Design.					

**RF TEST FIXTURE IMPEDANCE CHARACTERISTICS**

Frequency (MHz)	$Z_{IF}$ ( $\Omega$ )	$Z_{OF}$ ( $\Omega$ )
1090 (Actual + Optimal)	0.58-j0.58	0.79-j0.96
Impedance Definition		

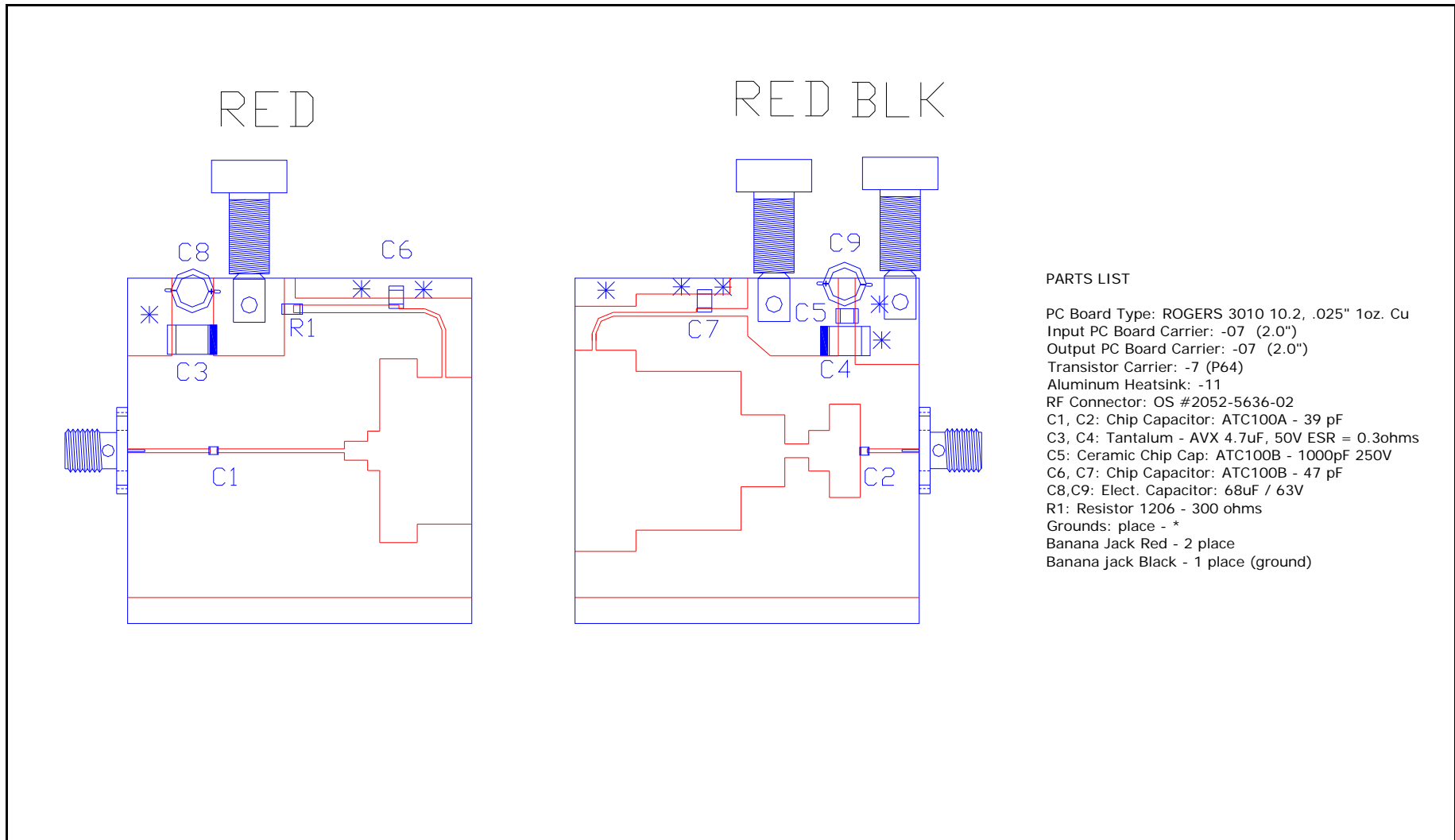
**PACKAGE DIMENSIONAL OUTLINE DRAWING**



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.380	0.390	9.65	9.90
B	0.035	0.045	0.89	1.14
C	1.335	1.345	33.90	34.16
D	0.139	0.166	3.53	4.21
E	0.123	0.133	3.12	3.37
F	1.095	1.105	27.81	28.06
G	0.057	0.067	1.44	1.70
H	0.170	0.210	4.32	5.33
I	0.170	0.210	4.32	5.33
J	0.003	0.006	0.08	0.15
K	0.495	0.505	12.57	12.82
L	0.364	0.374	9.24	9.49
M	0.772	0.788	19.60	20.01

PIN SCHEDULE	
D	DRAIN
S	SOURCE
G	GATE

**RF TEST FIXTURE – ASSEMBLY AND PARTS LIST**



**PARTS LIST**

- PC Board Type: ROGERS 3010 10.2, .025" 1oz. Cu
- Input PC Board Carrier: -07 (2.0")
- Output PC Board Carrier: -07 (2.0")
- Transistor Carrier: -7 (P64)
- Aluminum Heatsink: -11
- RF Connector: OS #2052-5636-02
- C1, C2: Chip Capacitor: ATC100A - 39 pF
- C3, C4: Tantalum - AVX 4.7uF, 50V ESR = 0.3ohms
- C5: Ceramic Chip Cap: ATC100B - 1000pF 250V
- C6, C7: Chip Capacitor: ATC100B - 47 pF
- C8,C9: Elect. Capacitor: 68uF / 63V
- R1: Resistor 1206 - 300 ohms
- Grounds: place - \*
- Banana Jack Red - 2 place
- Banana jack Black - 1 place (ground)

**DEFINITIONS**

<b>Data Sheet Status</b>	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
<b>Maximum Ratings</b>	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only. Operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

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