

Part Number: **ILD1011M400–ILD1011M400S**

Integra

TECHNOLOGIES, INC.

Avionics Band RF Power LDMOS FET

Available in a bolt down flanged version as ILD1011M400 or in a solder mount earless version ILD1011M400S. The high power transistor part number ILD1011M400 is designed for Avionics systems operating at 1030-1090 MHz. Operating at 50 μ s, 2% pulse conditions this LDMOS FET device supplies a minimum of 400 watts of power across the instantaneous operating bandwidth of 1030-1090 MHz. All devices are 100% screened for large signal RF parameters.



Silicon LDMOS FET

- High Power Gain
- Superior thermal stability

Class AB Operation

- Gate biased to $I_{DQ} = 50$ mA

Configuration

- Common Source

Gold Metal

- Maximum Reliability

Package

- Thermally enhanced
- Pb-free and RoHS-compliant

Epoxy Sealed Lid

- Gross Leak Qualified

RF Test Fixture

- Broadband
- Matched to 50 ohms
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning required

TYPICAL DATA TYPICAL DATA TYPICAL DATA TYPICAL DATA

Feq (MHz)	PIN (W)	RL (dB)	P _{OUT} (W)	G (dB)	Id (A)	nd (%)	Droop (dB)	VSWR-S 1.5:1 (P-F)	VSWR-S 3:1 (P-F)
1030	11.27	-18.0	400	15.50	23.55	59.2	-0.09	P	P
1090	10.21	-14.0	400	15.93	24.60	56.4	-0.10	P	P

MAXIMUM RATINGS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Drain-Source Voltage	V_{DS}	--	65	V	--
BD	Gate-Source Voltage	V_{GS}	-0.5	12	V	--
BD	Storage Temperature Range	T_{STG}	-55	+200	°C	--
BD	Operating Junction Temperature Range	T_J	-55	+200	°C	--
Note	Screen 'BD' = parameter qualified By Design.					

THERMAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	0.07	°C/W	$V_D=32V, I_{DQ}=50mA, T_F=25\pm5^\circ C, P_{OUT}=400W$
Note	Screen 'BD' = parameter qualified By Design.					

PROCESSING SPECIFICATIONS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

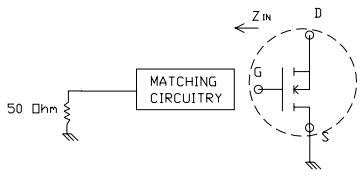
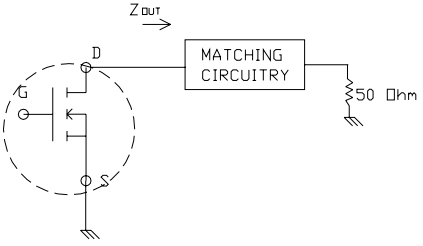
DC ELECTRICAL CHARACTERISTICS

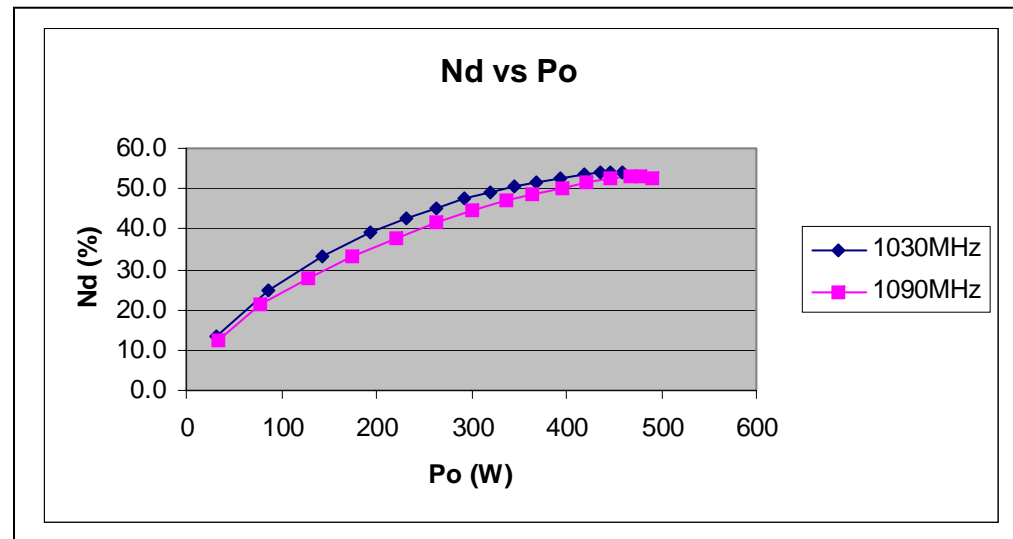
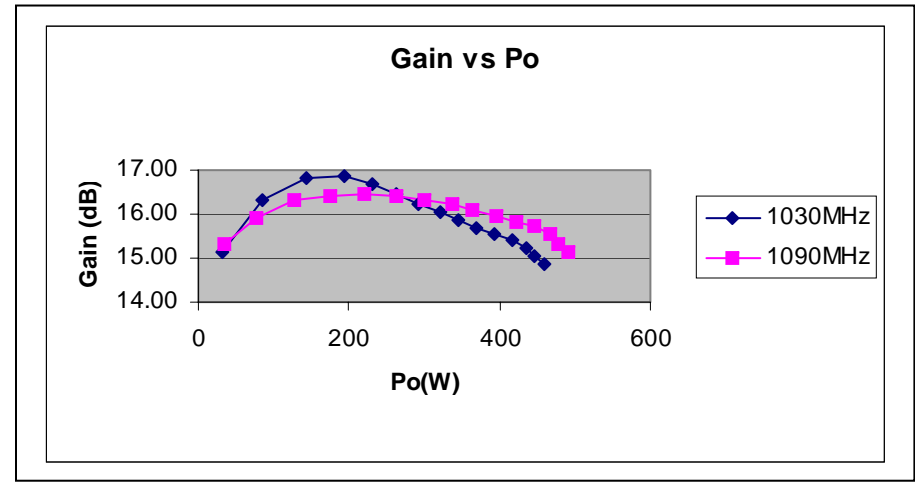
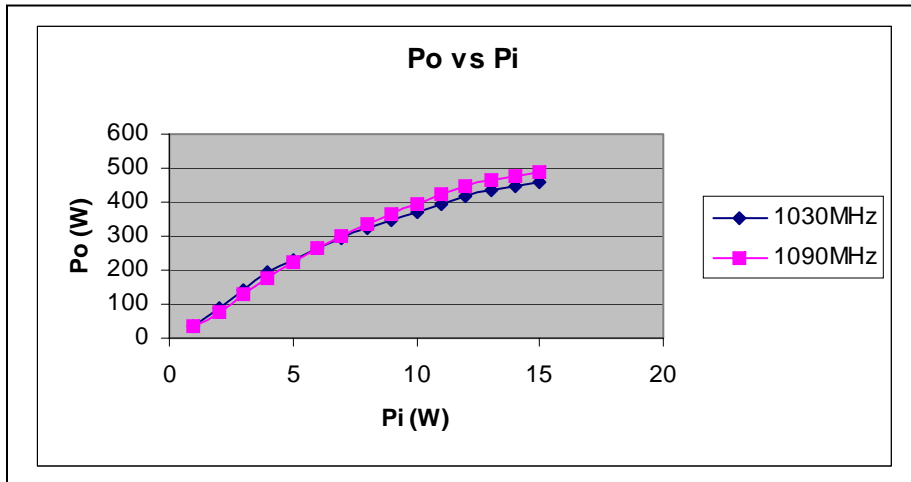
Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Drain-Source Breakdown Voltage	BV_{DSS}	65		V	$I_D = 30mA, V_{GS} = 0V, T_F = 25\pm5^\circ C$
100%	Drain Leakage Current	I_{DSS}		10	μA	$V_{DS} = 32V, V_{GS} = 0V, T_F = 25\pm5^\circ C$
100%	Gate Threshold Voltage	V_{GSTH2}	1.5	2.5	V	$I_D = 100mA, V_{GS} = 5V, T_F = 25\pm5^\circ C$
100%	Gate Leakage Current	I_{GSS}	--	1	μA	$V_{GS} = 5V, V_{DS} = 0V, T_F = 25\pm5^\circ C$

RF ELECTRICAL CHARACTERISTICS

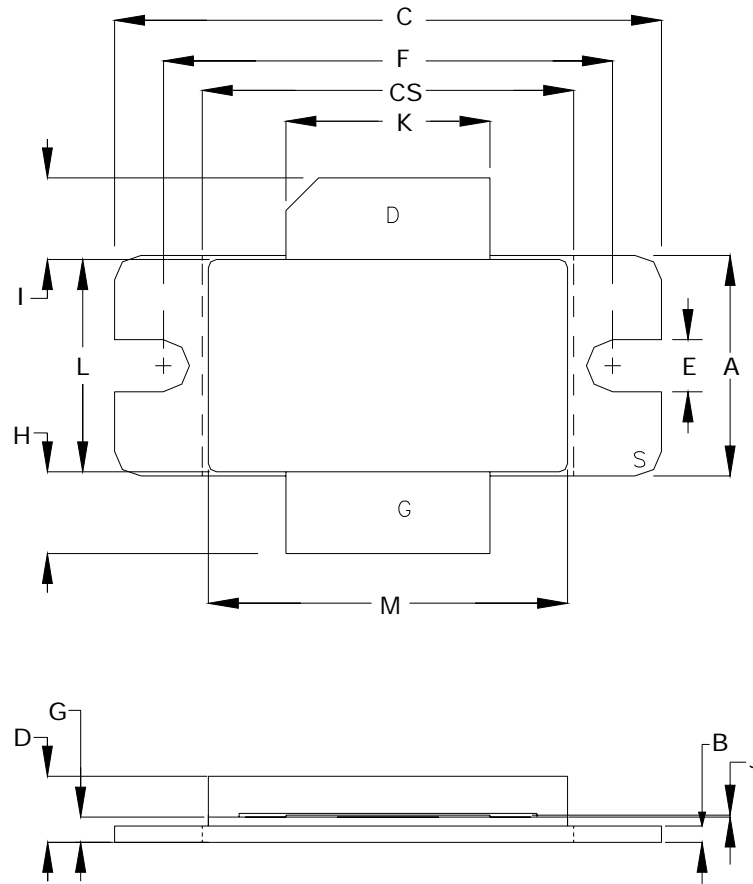
Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	RL	-18	-10	dB	$V_{DD}=32V, P_{OUT}=400W, \text{Pulse}=50\mu s, 2\%, T_F=25\pm 5^\circ C, F=F1, I_{DQ}=50mA.$
BD	Maximum Overdrive	$P_{IN(MAX)}$		20	W	$V_{DD}=32V, \text{Pulse}=50\mu s, 2\%, T_F=25\pm 5^\circ C, F=F1, I_{DQ}=50mA.$
100%	Power Gain	Gp	14	17.5	dB	$V_{DD}=32V, P_{OUT}=400W, \text{Pulse}=50\mu s, 2\%, T_F=25\pm 5^\circ C, F=F1, I_{DQ}=50mA.$
100%	Input Power	Pin	7.11	15.92	W	$V_{DD}=32V, P_{OUT}=400W, \text{Pulse}=50\mu s, 2\%, T_F=25\pm 5^\circ C, F=F1, I_{DQ}=50mA.$
100%	Drain Efficiency ($P_o/I_D/V_{DD}$)	N_d	45	75	%	$V_{DD}=32V, P_{OUT}=400W, \text{Pulse}=50\mu s, 2\%, T_F=25\pm 5^\circ C, F=F1, I_{DQ}=50mA.$
100%	Pulse Amplitude Droop	Droop	-0.3	+0.3	dB	$V_{DD}=32V, P_{OUT}=400 W, \text{Pulse}=50\mu s, 2\%, T_F=25\pm 5^\circ C, F=F1, I_{DQ}=50mA.$
100%	Stability into 1.5:1 VSWR	VSWR-S	--	--	--	$V_{DD}=32V, P_{OUT}=400 W, \text{Pulse}=50\mu s, 2\%, T_F=25\pm 5^\circ C, F=F1, I_{DQ}=50mA.$ Rotate 1.5:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse.
100%	Load Mismatch Tolerance	VSWR-LMT	--	3:1	--	$V_{DD}=32V, P_{OUT}=400 W, \text{Pulse}=50\mu s, 2\%, T_F=25\pm 5^\circ C, F=F1, I_{DQ}=50mA.$ Rotate 3:1 output VSWR through 360° phase. Survival.
BD	Pulse Risetime	RT	--	60	ns	$V_{DD}=32V, P_{OUT}=400 W, \text{Pulse}=50\mu s, 2\%, T_F=25\pm 5^\circ C, F=F1, I_{DQ}=50mA.$ Measure between 10% and 90% detected power points.
Note 1	F1 = 1030/1090 MHz.					
Note 2	Pulse format = 50μs, 2%					
Note 3	T_F = Device flange temperature.					
Note 4	Screen 'BD' = parameter qualified By Design.					

RF TEST FIXTURE IMPEDANCE CHARACTERISTICS

Frequency (MHz)	$Z_{IF} (\Omega)$	$Z_{OF} (\Omega)$
1030	4.35 - j1.80	1.28 - j0.56
1090	4.67 - j1.40	1.00 - j0.33
Impedance Definition		



PACKAGE DIMENSIONAL OUTLINE DRAWING

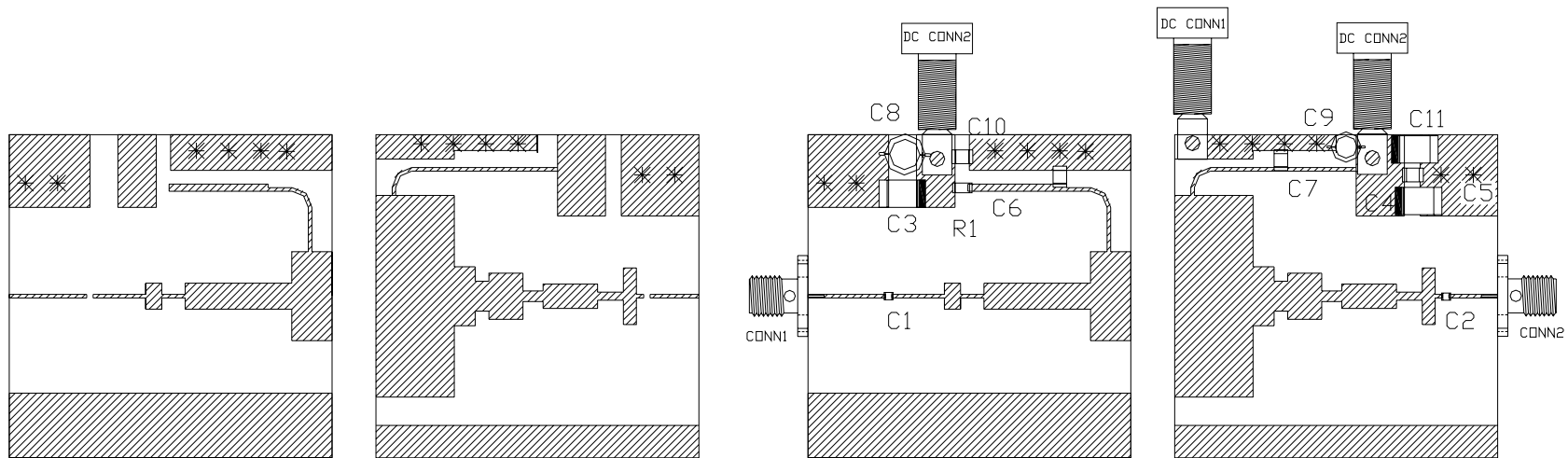


'S' VERSION USE DIM CS
NON 'S' VERSION USE DIM C

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.535	0.545	13.58	13.84
B	0.035	0.045	0.89	1.14
C	1.335	1.345	33.90	34.16
CS	0.905	0.915	22.99	23.24
D	0.147	0.177	3.73	4.50
E	0.123	0.133	3.12	3.37
F	1.095	1.105	27.81	28.06
G	0.057	0.067	--	--
H	0.170	0.210	4.32	5.33
I	0.170	0.210	4.32	5.33
J	0.003	0.006	0.08	0.15
K	0.495	0.505	12.57	12.82
L	0.514	0.524	13.05	13.31
M	0.871	0.889	22.12	22.58

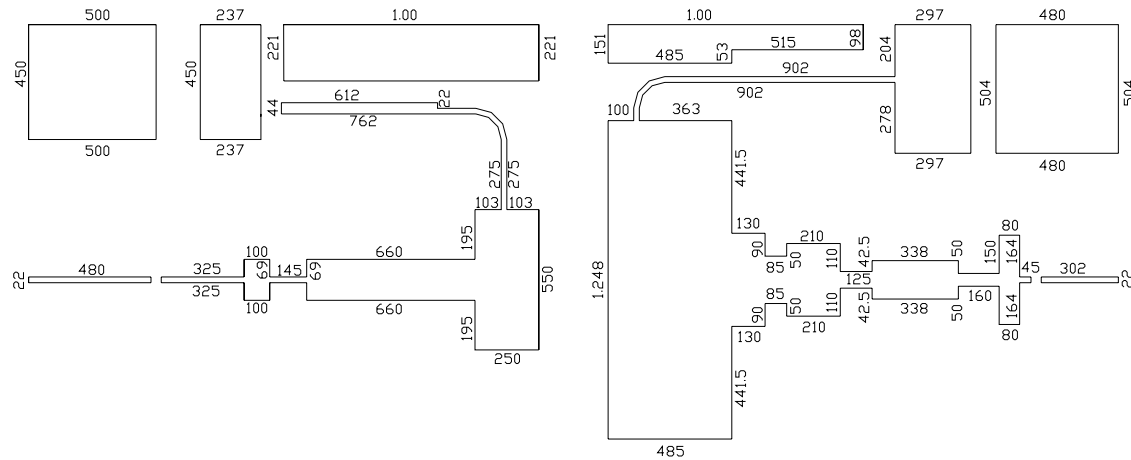
PIN SCHEDULE	
D	DRAIN
S	SOURCE
G	GATE

RF TEST FIXTURE – ASSEMBLY AND PARTS LIST

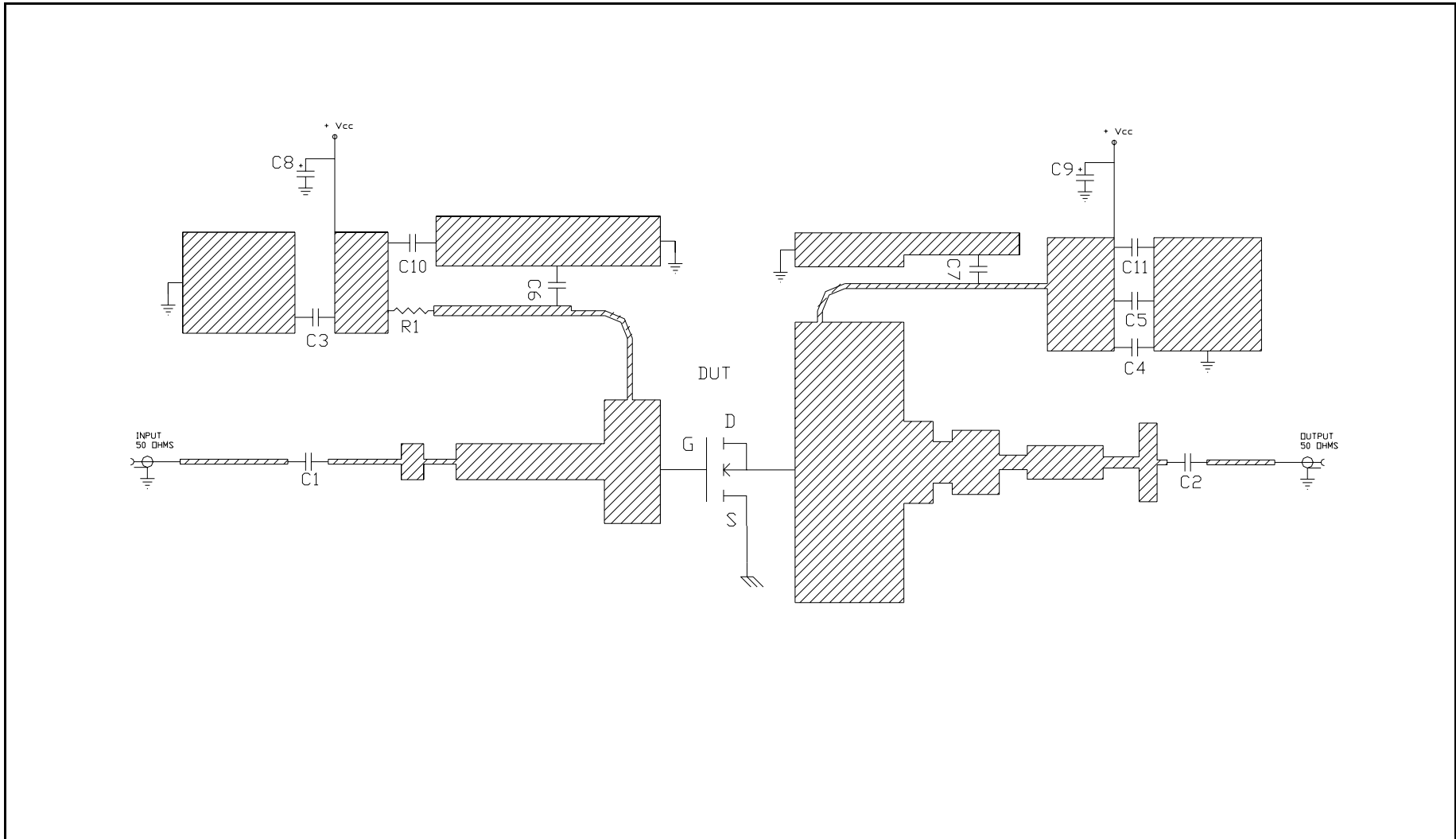


COMPONENT	DESCRIPTION
DUT	TRANSISTOR #ILD1011M400, MOUNT HARD TO THE RIGHT
PC BOARD	ROGERS #RD3010, TH=0.025" 1oz. Cu
C1, C2	CHIP CAPACITOR, TYPE ATC100A, 39 pF
C3, C4, C11	TANTALUM AVX 4.7uF, 50V ESR = 0.3 ohms
C5, C10	CERAMIC CHIP CAPACITOR ATC100B 1000pF 250V
C6, C7	CAPACITOR CHIP ATC100B 47pF
C8, C9	ELECTROLYTIC CAPACITOR 68uF/63V
R1	RESISTOR SIZE 1206 - 300 ohms
GS	GROUND SHIM, COPPER, TH=0.001"
CONN1, CONN2	SMA CONNECTOR, TYPE DS #2052-5636-02
INPUT PC BOARD CARRIER	2 INCH BRASS - 07 (2.00")
OUTPUT PC BOARD CARRIER	2 INCH BRASS - 07 (2.00")
TRANSISTOR CARRIER	2 INCH COPPER - 16
TRANSISTOR CLAMP	INDRYL CLAMP - 12
HEATSINK	2 INCH HEATSINK - 11
DC CONN1	BANANA JACK, BLACK
DC CONN2	BANANA JACK, RED
DC CONN3	BANANA JACK, YELLOW
NOTE	FIXTURE HARDWARE DRAWINGS AVAILABLE ON REQUEST

RF TEST FIXTURE – CIRCUIT DIMENSIONS IN MILS



RF TEST FIXTURE – ELECTRICAL SCHEMATIC



DEFINITIONS

Data Sheet Status	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
Maximum Ratings	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only. Operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

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