# Part Number: ILD1214EL100 (Preliminary)

Integra
TECHNOLOGIES, INC.

## L-Band RF Power LDMOS Transistor

The high power pulsed transistor part number ILD1214EL100 is designed for L-Band systems operating at 1.215–1.400 GHz. Operating at a pulse width of 16ms with a duty factor of 50%, this dual LDMOS device 100 watts of peak pulse power across the instantaneous operating bandwidth of 1.215-1.400 GHz. Fabricated with all gold metal contact, wire bonding and package for maximum reliability. All devices are 100% screened for large signal RF parameters in the broadband RF test fixture across the entire specified operating bandwidth with no variable or external tuning.


**Silicon LDMOS**
- High Power Gain
- Superior Thermal Stability

**Class AB Operation**
- Gate biased to $I_{DQ}$=250mA

**Configuration**
- Common Source

**Gold Metal**
- Gold Chip Metal
- Gold Wire Bond
- Maximum Reliability

**Package**
- Thermally Enhanced
- Gold Metal Based

**Epoxy Sealed Lid**
- Gross Leak Qualified

**RF Test Fixture**
- Broadband
- Matched to 50Ω
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning required

***PRELIMINARY BROADBAND DATA***

**TBD**



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## MAXIMUM RATINGS

| Screen | Parameter | Symbol | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| BD | Drain-Source Voltage | $V_{DS}$ | -- | 65 | V | -- |
| BD | Gate-Source Voltage | $V_{GS}$ | -0.5 | +12 | V | -- |
| BD | Storage Temperature Range | $T_{STG}$ | -40 | +150 | °C | -- |
| BD | Operating Junction Temperature Range | $T_J$ | -55 | +200 | °C | -- |
| | | | | | | |
| Note | Screen 'BD' = parameter qualified By Design. | | | | | |

## THERMAL CHARACTERISTICS

| Screen | Parameter | Symbol | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| BD | Thermal Resistance | $R_{TH(JC)}$ | -- | TBD | °C/W | $V_{dd}$=30V, $I_{DQ}$=250mA, $T_F$=70±5°C, $P_{OUT}$=100W |
| | | | | | | |
| Note | Screen 'BD' = parameter qualified By Design. | | | | | |

## PROCESSING SPECIFICATIONS

| Screen | Parameter | Symbol | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| 100% | DC Wafer Probe | -- | -- | -- | -- | Per Integra specification. |
| Q1 | Wafer DC and RF Qualification | -- | -- | -- | -- | Per Integra specification. |
| LM | Wire Bond Strength | -- | -- | -- | -- | Line monitor per Integra specification. |
| 100% | Pre-cap visual inspection | -- | -- | -- | -- | Per Integra specification |
| 100% | Gross leak test | -- | -- | -- | -- | MIL-STD-750D, Method 1071, Test Condition C |
| | | | | | | |
| Note | Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer. | | | | | |
| Note | Screen 'LM' = parameter is qualified by assembly line monitor. | | | | | |

## DC ELECTRICAL CHARACTERISTICS

| Screen | Parameter | Symbol | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| 100% | Drain-Source Breakdown Voltage (each side) | $BV_{DSS}$ | 65 | -- | V | $I_D$ = 10mA, $V_{GS}$ = 0V, $T_F$ = 25±5°C |
| BD | Drain Leakage Current (each side) | $I_{DSS}$ | -- | 1.0 | µA | $V_{DS}$ = 30V, $V_{GS}$ = 0V, $T_F$ = 25±5°C |
| 100% | Gate Threshold Voltage (each side) | $V_{GSTH2}$ | 2.0 | 3.0 | V | $I_D$ = 0.75A, $V_{DS}$ = 30V, $T_F$ = 25±5°C |
| BD | Gate Leakage Current (each side) | $I_{GSS}$ | -- | 1.0 | µA | $V_{GS}$ = 10V, $V_{DS}$ = 0V, $T_F$ = 25±5°C |



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## RF ELECTRICAL CHARACTERISTICS

| Screen | Parameter | Symbol | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| 100% | Input Return Loss | RL | -18 | -7 | dB | $V_{DD}$=V1; $I_{DQ}$=$I_{DQ1}$: $T_F$=$T_{F1}$: $P_O$=$P_{OUT1}$: F=F1, F2, F3: PW1,DF1 |
| 100% | Power Gain | $G_P$ | 10 | 16.5 | dB | $V_{DD}$=V1; $I_{DQ}$=$I_{DQ1}$: $T_F$=$T_{F1}$: $P_O$=$P_{OUT1}$: F=F1, F2, F3: PW1,DF1 |
| 100% | Input Power | Pi | 2.24 | 10.0 | W | $V_{DD}$=V1; $I_{DQ}$=$I_{DQ1}$: $T_F$=$T_{F1}$: $P_O$=$P_{OUT1}$: F=F1, F2, F3: PW1,DF1 |
| 100% | Drain Current Efficiency | $N_D$ | 38 | 75 | % | $V_{DD}$=V1; $I_{DQ}$=$I_{DQ1}$: $T_F$=$T_{F1}$: $P_O$=$P_{OUT1}$: F=F1, F2, F3: PW1,DF1 |
| 100% | Pulse Amplitude Droop | Droop | -0.5 | 0.5 | dB | $V_{DD}$=V1; $I_{DQ}$=$I_{DQ1}$: $T_F$=$T_{F1}$: $P_O$=$P_{OUT1}$: F=F1, F2, F3: PW1,DF1 |
| 100% | Gain Flatness versus Frequency | GF | 0 | 1.5 | dB | $V_{DD}$=V1; $I_{DQ}$=$I_{DQ1}$: $T_F$=$T_{F1}$: $P_O$=$P_{OUT1}$: F=F1, F2, F3: PW1,DF1 |
| 100% | Stability into 2:1 VSWR | VSWR-S | 2:1 | -- | -- | $V_{DD}$=V1; $I_{DQ}$=$I_{DQ1}$: $T_F$=$T_{F1}$: $P_O$=$P_{OUT1}$: F=F1, F2, F3: PW1,DF1<br>Rotate 2:1 output VSWR through 360° phase.<br>No oscillatory or pulse break-up characteristics allowed on detected output pulse. |
| 100% | Load Mismatch Tolerance | LMT | TBD | -- | -- | $V_{DD}$=V1; $I_{DQ}$=$I_{DQ1}$: $T_F$=$T_{F1}$: $P_O$=$P_{OUT1}$: F=F1, F2, F3: PW1,DF1<br>Rotate output VSWR through 360° phase.<br>Post test $P_O$ = Pre test $P_O$±10W. |
| Notes | V1=30V; $I_{DQ1}$ (Drain Quiescent Current)=250mA<br>PW1(Pulse Width 1) =16ms; DF1(Duty Factor 1)=50%;<br>$P_{OUT1}$=100W; F1=1.215GHz, F2=1.300GHz, F3=1.400GHz<br>$T_{F1}$ (Flange Temp)=40±5°C;<br>RF Electrical characteristics are tested in broadband RF test fixture. Thermal grease is applied to the flange for RF testing. | | | | | |

## BROADBAND RF TEST FIXTURE IMPEDANCE CHARACTERISTICS

| Frequency (GHz) | $Z_{IF}$ (Ω) | $Z_{OF}$ (Ω) |
|---|---|---|
| 1.215 | TBD | TBD |
| 1.300 | TBD | TBD |
| 1.400 | TBD | TBD |

$Z_{IF}$ = The test fixture input impedance.

$Z_{OF}$= The test fixture output impedance.



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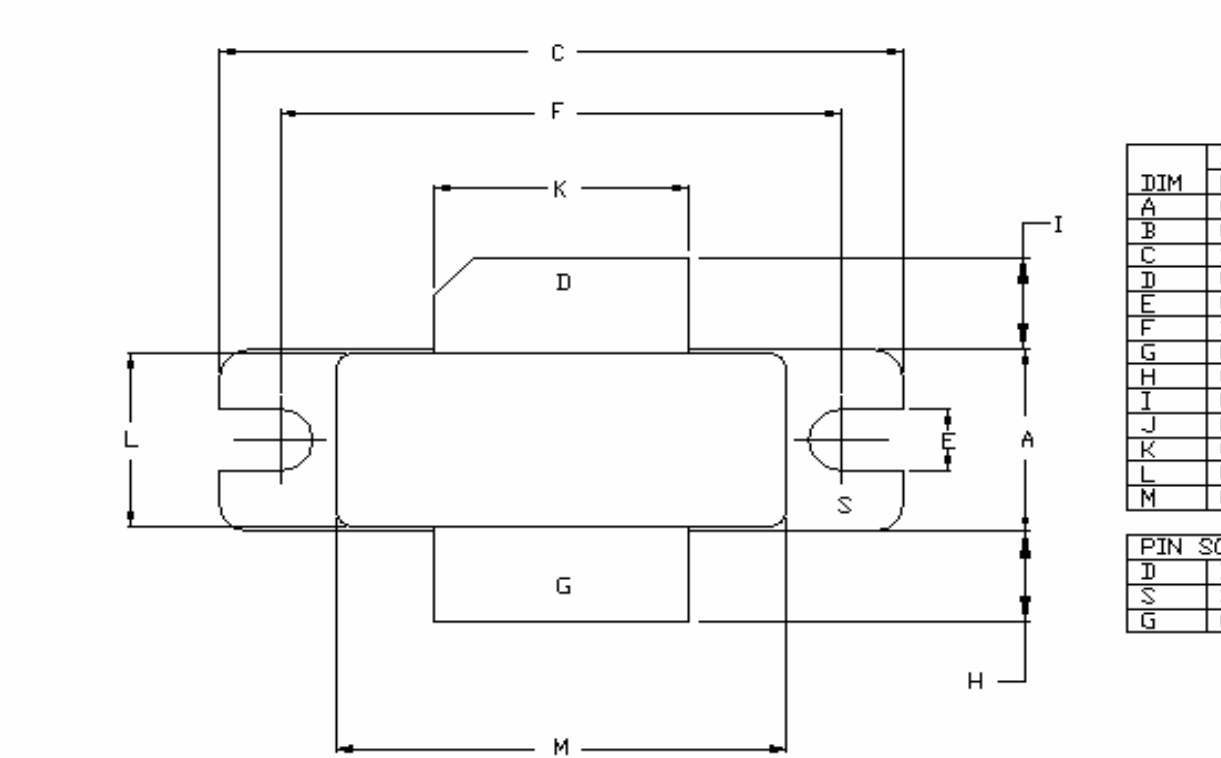
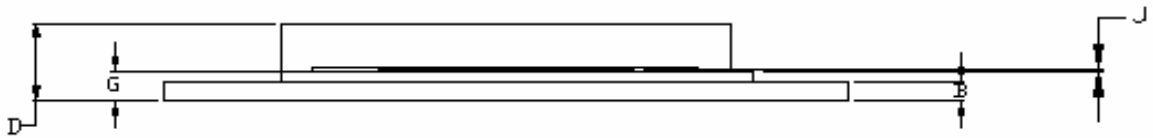
**PACKAGE DIMENSIONAL OUTLINE DRAWING**




| DIM | INCHES MIN | INCHES MAX | MILLIMETERS MIN | MILLIMETERS MAX |
|---|---|---|---|---|
| A | 0.380 | 0.390 | 9.65 | 99.0 |
| B | 0.035 | 0.045 | 0.88 | 1.14 |
| C | 1.335 | 1.345 | 33.90 | 34.16 |
| D | 0.127 | 0.157 | 3.22 | 3.98 |
| E | 0.123 | 0.133 | 3.12 | 3.37 |
| F | 1.095 | 1.105 | 27.81 | 28.0 |
| G | 0.057 | 0.067 | 1.44 | 1.70 |
| H | 0.170 | 0.210 | 4.32 | 5.33 |
| I | 0.170 | 0.210 | 4.32 | 5.33 |
| J | 0.049 | 0.075 | 1.24 | 1.90 |
| K | 0.495 | 0.505 | 12.57 | 12.82 |
| L | 0.364 | 0.374 | 9.24 | 9.49 |
| M | 0.875 | 0.885 | 22.22 | 22.47 |

| PIN SCHEDULE | |
|---|---|
| D | DRAIN |
| S | SOURCE |
| G | GATE |



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**RF-TEST-FIXTURE ASSEMBLY AND PART LIST**

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**RF-TEST-FIXTURE CIRCUIT DIMENSIONS**

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**RF-TEST-FIXTURE ELECTRICAL SCHEMATIC**

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## DEFINITIONS

| Data Sheet Status | |
|---|---|
| Proposed Specification | This data sheet contains proposed specifications. |
| Preliminary Specification | This data sheet contains specifications based on preliminary measurements and data. |
| Product Specification | This data sheet contains final product specifications. |
| | |
| **Maximum Ratings** | |
| Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only. Operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability. | |

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