Part Number: ILD1214EL40

Integra
TECHNOLOGIES, INC.

L-Band Radar Transistor

Part number ILD1214EL40 is designed for L-Band radar applications operating over the 1.215-1.400 GHz instantaneous frequency band. Under 5ms/20% pulsing conditions it easily supplies a minimum of 40 watts of peak output power with over 12db gain. Since it operates under Class B or AB bias it exhibits a fairly linear Pin versus Pout transfer characteristic, which allows operation at reduced output power levels. All devices are 100% screened for large signal RF parameters in a fixed tuned broadband matching circuit / test fixture. The use of external tuners is not allowed during screening.

Silicon LDMOS FET
- High Power Gain
- Excellent thermal stability
- Gold Metal

Gold Metal System
- Complete Gold System
- LDMOS with Gold Metal
- Gold Bond Wires
- Gold Package Metal
- Maximum Reliability

Class B, AB, or A Operation
- Linearized Transfer Characteristic

BeO Free Package
- Metal Based
- Epoxy Seal

High Power RF Test / Fixture
- Broadband
- Matched to 50 Ω (ohms)
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning required

TYPICAL DATA TYPICAL DATA TYPICAL DATA TYPICAL DATA

Device	Freq (GHz)	PW (ms)	Duty (%)	V_{ds} (V)	P_{IN} (W)	IRL (dB)	P_{OUT} (W)	G_p (dB)	I_d (A)	nd (%)	Droop (dB)
D4412-1	1.215	5	20	30	1.80	-13	47	13.9	3.24	48	-0.15
	1.215	5	20	30	1.30	-13	38	14.3	2.96	42	-0.14
	1.215	5	20	30	1.20	-13	33	14.4	2.72	40	-0.13
	1.300	5	20	30	1.70	-13	43	14.0	3.10	46	-0.15
	1.300	5	20	30	1.50	-13	40	14.2	3.00	44	-0.15
	1.300	5	20	30	1.20	-12	32	14.3	2.70	40	-0.14
	1.400	5	20	30	1.90	-11	49	14.3	2.80	58	-0.08
	1.400	5	20	30	1.40	-11	41	15.0	2.60	53	-0.08
	1.400	5	20	30	1.20	-11	39	15.1	2.51	52	-0.08

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MAXIMUM RATINGS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Drain-Source Voltage	V_{DS}	--	65	V	--
BD	Gate-Source Voltage	V_{GS}	-0.5	12	V	--
BD	Storage Temperature Range	T_{STG}	-55	+150	°C	--
BD	Operating Junction Temperature Range	T_J	-55	+200	°C	--
Note	Screen 'BD' = parameter qualified By Design.					

THERMAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	1.2	°C/W	V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=25±5°C, P_{OUT}=40W, F=F3
Note	Screen 'BD' = parameter qualified By Design.					

PROCESSING SPECIFICATIONS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071.6, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

DC ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Drain-Source Breakdown Voltage	BV_{DSS}	65	--	V	I_{DS}=10mA, V_{GS}=0V, T_F=25±5°C
100%	Drain Leakage Current	I_{DSS}	--	1.0	uA	V_{DS}=28V, V_{GS}=0V, T_F=25±5°C
100%	Operating Gate Voltage	V_{GS}	2.0	4	V	V_{DS}=5V, I_D=0.1A, T_F=25±5°C
100%	Gate Leakage Current	I_{GSS}	--	1.0	uA	V_{GS}=10V, V_{DS}=0V, T_F=25±5°C

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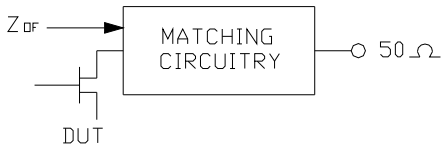
RF ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	IRL	-18	-7	dB	V_{DD}=V1, I_{DQ}= I_{DQ1}, T_F=T_{F1}, P_O=P_{OUT1}, F=F1, F2, F3, PW=PW1, DF=DF1
100%	Input Power	P_i	0.80	2.52	W	V_{DD}=V1, I_{DQ}= I_{DQ1}, T_F=T_{F1}, F=F1, F2, F3, PW=PW1, DF=DF1
100%	Power Gain	G_P	12	17	dB	V_{DD}=V1, I_{DQ}= I_{DQ1}, T_F=T_{F1}, P_O=P_{OUT1}, F=F1, F2, F3, PW=PW1, DF=DF1
100%	Drain Efficiency	N_D	33	75	%	V_{DD}=V1, I_{DQ}= I_{DQ1}, T_F=T_{F1}, P_O=P_{OUT1}, F=F1, F2, F3, PW=PW1, DF=DF1
100%	Pulse Amplitude Droop	Drp	-0.5	0.5	dB	V_{DD}=V1, I_{DQ}= I_{DQ1}, T_F=T_{F1}, P_O=P_{OUT1}, F=F1, F2, F3, PW=PW1, DF=DF1
100%	Gain Flatness versus Frequency	GF	0	1.5	dB	V_{DD}=V1, I_{DQ}= I_{DQ1}, T_F=T_{F1}, P_O=P_{OUT1}, F=F1, F2, F3, PW=PW1, DF=DF1
100%	3:1 Load Mismatch Stability & Tolerance	VSWR-ST	--	--	--	V_{DD}=V1, I_{DQ}= I_{DQ1}, T_F=T_{F1}, P_O=P_{OUT1}, F=F1, F2, F3, PW=PW1, DF=DF1 Rotate 3:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse.
Note 1	V1 (Drain Supply Voltage) = 30V; I_{DQ1} (Drain Quiescent Current) = 100mA; PW1 (Pulse Width 1) = 5ms; DF1 (Duty Factor 1) = 20%.					
Note 2	Output Power Test Level: P_{OUT1} = 40W.					
Note 3	Test Frequencies: F1 = 1.215 GHz, F2 = 1.3 GHz, F3 = 1.4 GHz.					
Note 4	T_{F1} = 25±5°C = Device flange temperature.					
Note 5	Screen 'BD' = parameter qualified By Design.					
Note 6	RF Electrical characteristics in broadband RF test fixture.					

RF TEST FIXTURE IMPEDANCE CHARACTERISTICS

Frequency (GHz)	Z_{IF} (Ω)	Z_{OF} (Ω)
1.215	2.4 –j2.3	2.2 +j0.2
1.300	2.6 –j1.5	2.2 +j0.4
1.400	3.2 -j0.5	2.0 +j0.7
Impedance Definition		

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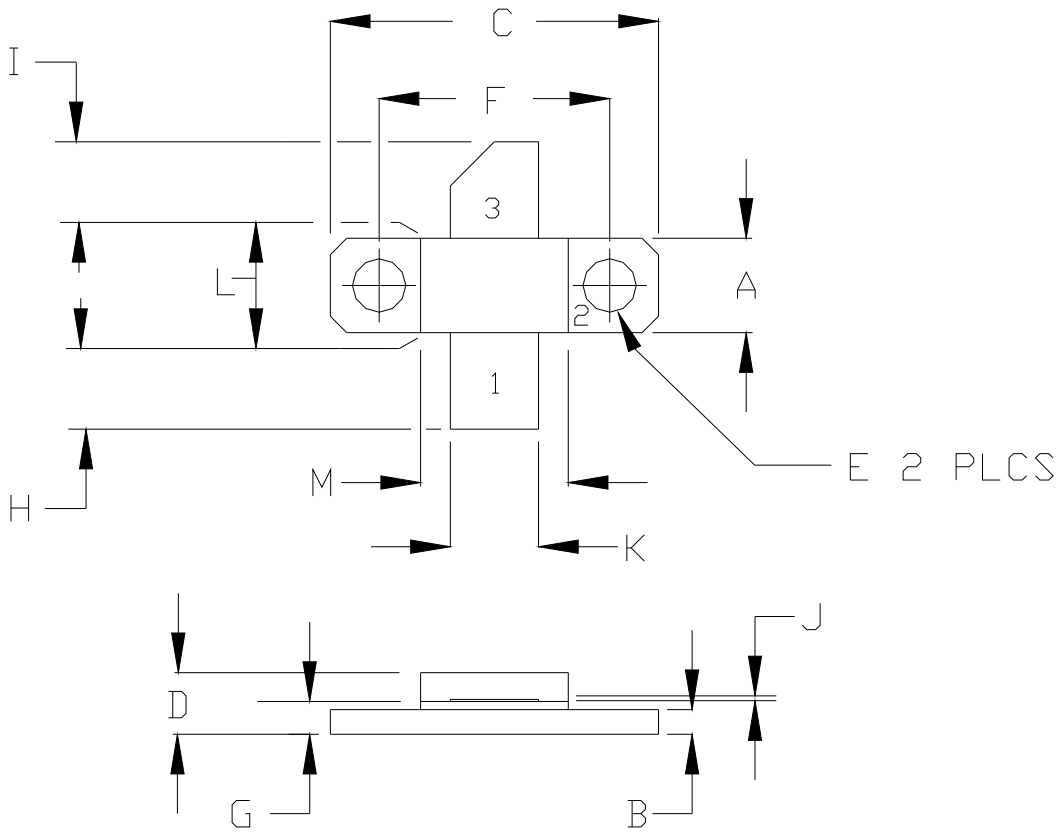
PACKAGE DIMENSIONAL OUTLINE DRAWING



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.225	0.235	5.71	5.96
B	0.055	0.065	1.40	1.65
C	0.795	0.805	20.19	20.44
D	0.140	0.160	3.55	4.06
E	0.125	0.135	3.18	3.43
F	0.557	0.567	14.14	14.40
G	0.050	0.070	1.27	1.77
H	0.215	0.245	5.46	6.22
I	0.215	0.245	5.46	6.22
J	0.004	0.006	0.10	0.15
K	0.210	0.220	5.33	5.58
L	0.225	0.235	5.71	5.96
M	0.355	0.365	9.01	9.27

PIN SCHEDULE	
1	GATE
2	SOURCE
3	DRAIN

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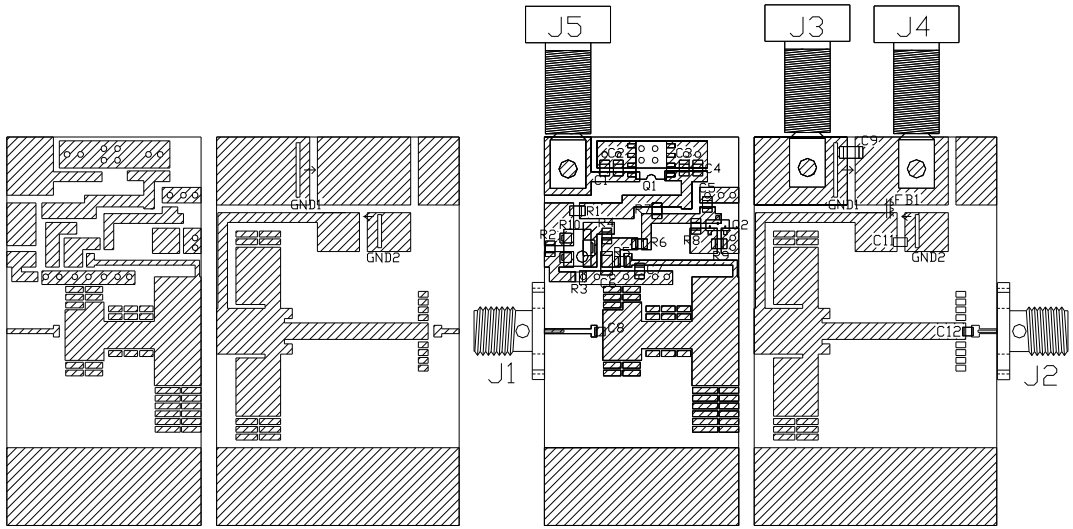
RF TEST FIXTURE – ASSEMBLY AND PARTS LIST



COMPONENT	DESCRIPTION
DUT	TRANSISTOR #ILD1214EL40 MOUNT HARD TO THE RIGHT
PC BOARD	ROGERS #RO 6010.2, 25 MILS THICK
C1, C4, C6, C9	CHIP CAPACITOR 1uF, 1206 MURATA GRM31CR72A105KA01L
C2, C3, C5, C7, C11, C12	CHIP CAPACITOR 0505, 33pF ATC 100A
C13 (EXTERNAL)	ELECTROLYTIC CAPACITOR, 4700uF / 50V
Q1	LM78L08
Q2	MMBT2222A FAIRCHILD SEMICONDUCTOR
R1	RESISTOR 820, 0805 (821)
R2	RESISTOR 390, 0805 (391)
R3	RESISTOR 150, 0805 (151)
R4	RESISTOR 1.8K, 0805 (182)
R5	RESISTOR 5R1, 0805 (5.1)
R6	RESISTOR 10K, 0805 (103)
R7	RESISTOR 1K, 0805 (102)
R8	RESISTOR 8.2K, 0805 (822)
R9	RESISTOR 1.5K, 0805 (152)
R10	RESISTOR POT, 200 #3224W-1-201E

COMPONENT	DESCRIPTION
GS PLATED THROUGH VIAS	GROUND SHIM, COPPER, TH=0.001"
J1, J2	SMA CONNECTOR, DS #2052-5636-02
INPUT PC BOARD CARRIER	2 INCH BRASS-3 (1")
OUTPUT PC BOARD CARRIER	2 INCH BRASS-4 (1.25")
TRANSISTOR CARRIER	2 INCH COPPER-05
TRANSISTOR CLAMP	NORYL CLAMP-TBD
ALUMINUM HEAT SINK	2 INCH HEATSINK-11
J3	BANANA JACK, BLACK
J4	BANANA JACK, RED
J5	BANANA JACK, BLUE
NOTE	FIXTURE HARDWARE DRAWINGS AVAILABLE ON REQUEST

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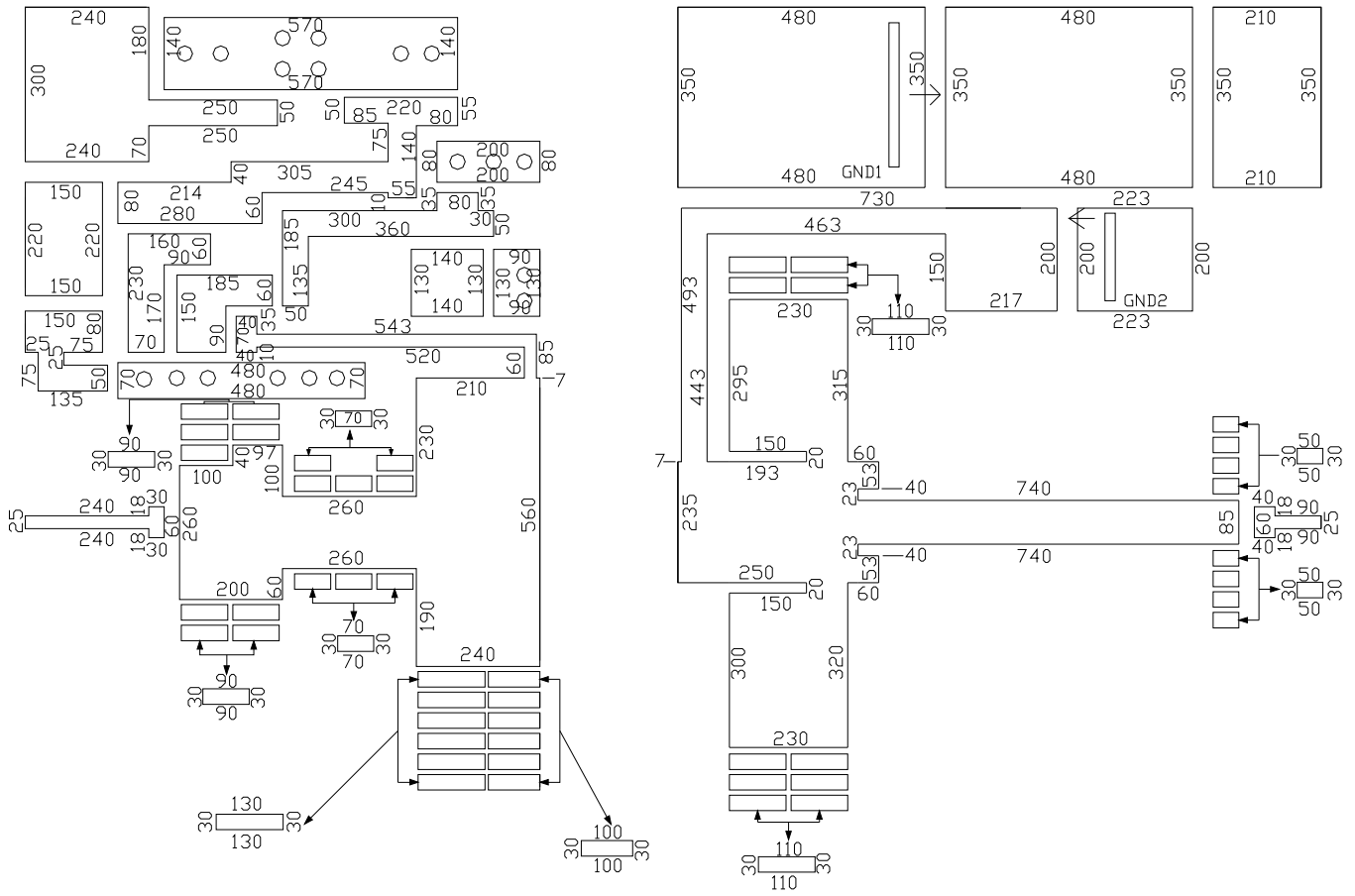
RF TEST FIXTURE – CIRCUIT DIMENSIONS IN MILS



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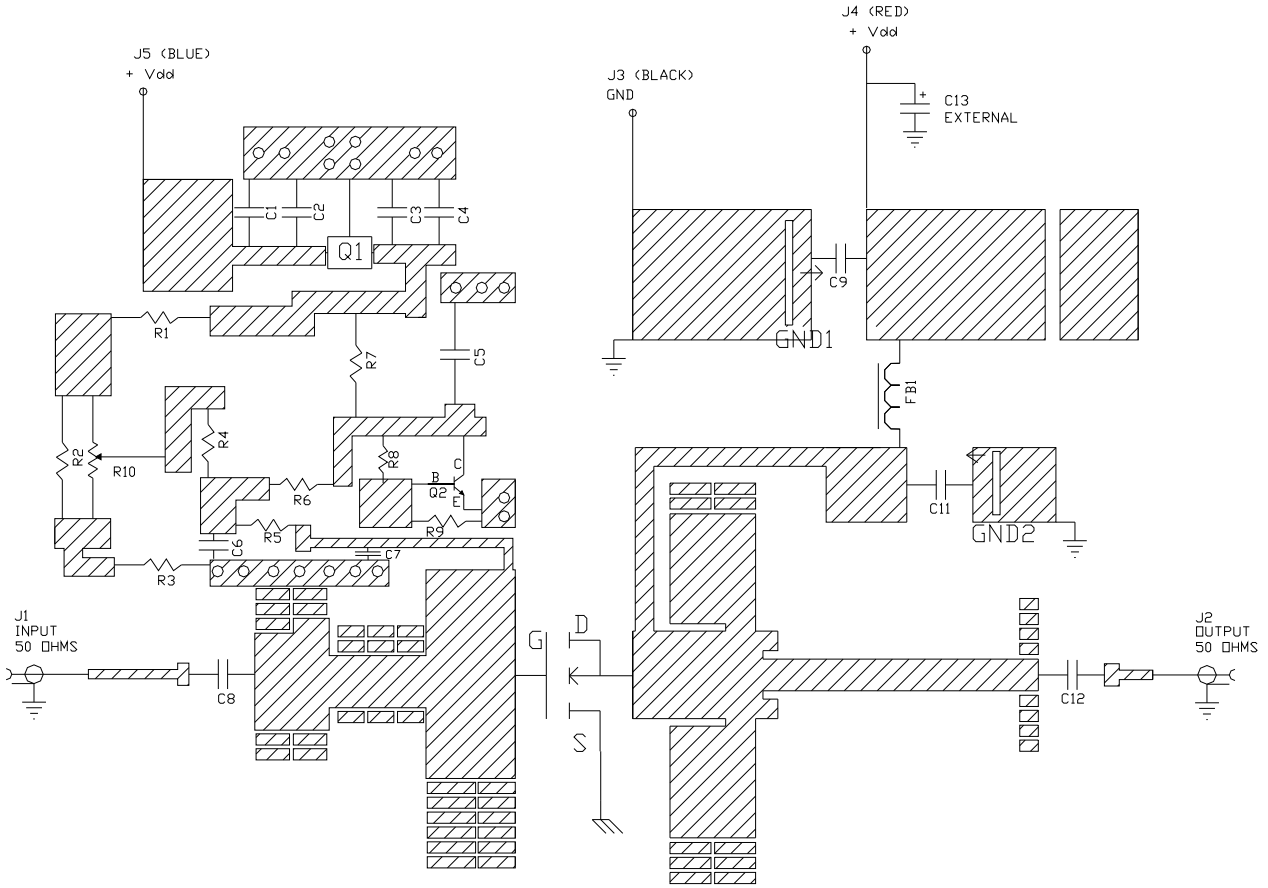
RF TEST FIXTURE – ELECTRICAL SCHEMATIC



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DEFINITIONS

Data Sheet Status	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.

Maximum Ratings

Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.

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