

## S-Band Radar Transistor

Part number ILD2731M140 is designed for S-Band radar applications operating over the 2.7 – 3.1 GHz instantaneous frequency band. Under 300us / 10% pulsed conditions it supplies a minimum of 140 watts of peak output power. Specified operation is with Class AB bias. The broadband test fixture includes a temperature compensated bias network. All devices are 100% screened for large signal RF parameters in a fixed tuned broadband matching circuit / test fixture. This device is rated for a peak output power level of  $P_{PEAK} = 140W @ 10\%$  duty factor. This corresponds to an average power  $P_{AVG} = 14W$ .



### Silicon LDMOS FET

- High Power Gain
- Excellent thermal stability
- Gold Metal

### Gold Metal System

- Complete Gold System
- LDMOS with Gold Metal
- Gold Bond Wires
- Gold Package Metal
- Maximum Reliability

### Class AB Operation

- Specified with AB bias

### Internal Impedance Matching

- Ease of Use
- Ultra Low Loss Design

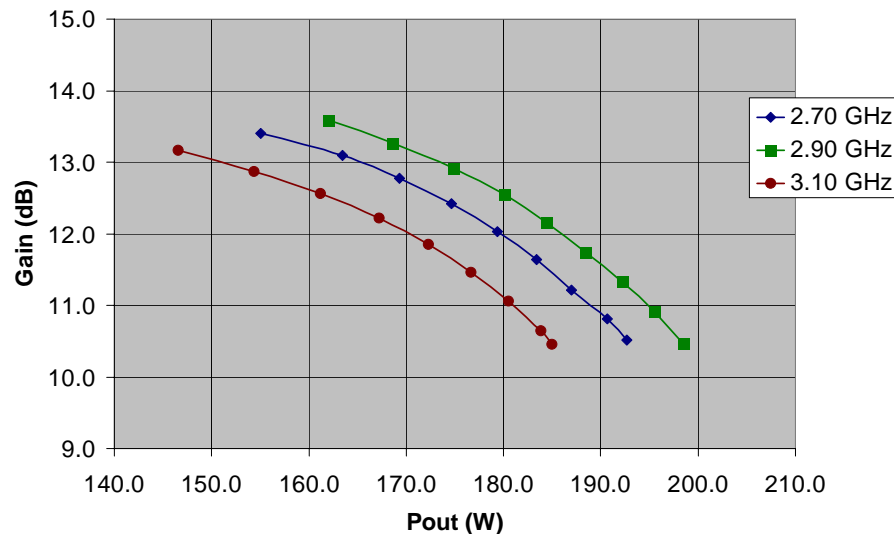
### BeO Free Package

- Metal Based
- Epoxy Seal

### High Power RF Test / Fixture

- Broadband
- Matched to 50  $\Omega$  (ohms)
- Temperature Compensated Bias
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning required

## GAIN VERSUS OUTPUT POWER



**MAXIMUM RATINGS**

| Screen | Parameter                                    | Symbol    | Min  | Max  | Units | Test Conditions             |
|--------|--|-----------|------|------|-------|-----------------------------|
| BD     | Drain-Source Voltage                         | $V_{DS}$  | --   | 65   | V     | --                          |
| BD     | Gate-Source Voltage                          | $V_{GS}$  | -0.5 | 12   | V     | --                          |
| BD     | Storage Temperature Range                    | $T_{STG}$ | -55  | +150 | °C    | --                          |
| BD     | Operating Junction Temperature Range         | $T_J$     | -55  | +200 | °C    | --                          |
| BD     | CW Operation                                 | --        | --   | --   | --    | Not rated for CW operation. |
| Note   | Screen 'BD' = parameter qualified By Design. |           |      |      |       |                             |

**THERMAL CHARACTERISTICS**

| Screen | Parameter                                    | Symbol       | Min | Max  | Units | Test Conditions  |
|--------|--|--------------|-----|------|-------|--|
| BD     | Thermal Resistance                           | $R_{TH(JC)}$ | --  | 0.17 | °C/W  | $V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{OUT}=140W.$ |
| Note   | Screen 'BD' = parameter qualified By Design. |              |     |      |       |  |

**PROCESSING SPECIFICATIONS**

| Screen | Parameter  | Symbol | Min | Max | Units | Test Conditions                               |
|--------|--|--------|-----|-----|-------|---|
| 100%   | DC Wafer Probe   | --     | --  | --  | --    | Per Integra specification.                    |
| Q1     | Wafer DC and RF Qualification  | --     | --  | --  | --    | Per Integra specification.                    |
| LM     | Wire Bond Strength   | --     | --  | --  | --    | Line monitor per Integra specification.       |
| 100%   | Pre-cap visual inspection  | --     | --  | --  | --    | Per Integra specification                     |
| 100%   | Gross leak test  | --     | --  | --  | --    | MIL-STD-750D, Method 1071.6, Test Condition C |
| Note   | Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer. |        |     |     |       |   |
| Note   | Screen 'LM' = parameter is qualified by assembly line monitor.                           |        |     |     |       |   |



**DC ELECTRICAL CHARACTERISTICS**

| Screen | Parameter                      | Symbol     | Min | Max | Units | Test Conditions                              |
|--------|--------------------------------|------------|-----|-----|-------|--|
| 100%   | Drain-Source Breakdown Voltage | $BV_{DSS}$ | 65  | --  | V     | $I_{DS}=10mA, V_{GS}=0V, T_F=25\pm5^\circ C$ |
| 100%   | Drain Leakage Current          | $I_{DSS}$  | --  | 10  | uA    | $V_{DS}=32V, V_{GS}=0V, T_F=25\pm5^\circ C$  |
| 100%   | Operating Gate Voltage         | $V_{GS}$   | 2.5 | 4.0 | V     | $V_{DS}=5V, I_D=100mA, T_F=25\pm5^\circ C$   |
| 100%   | Gate Leakage Current           | $I_{GSS}$  | --  | 1.0 | uA    | $V_{GS}=10V, V_{DS}=0V, T_F=25\pm5^\circ C$  |

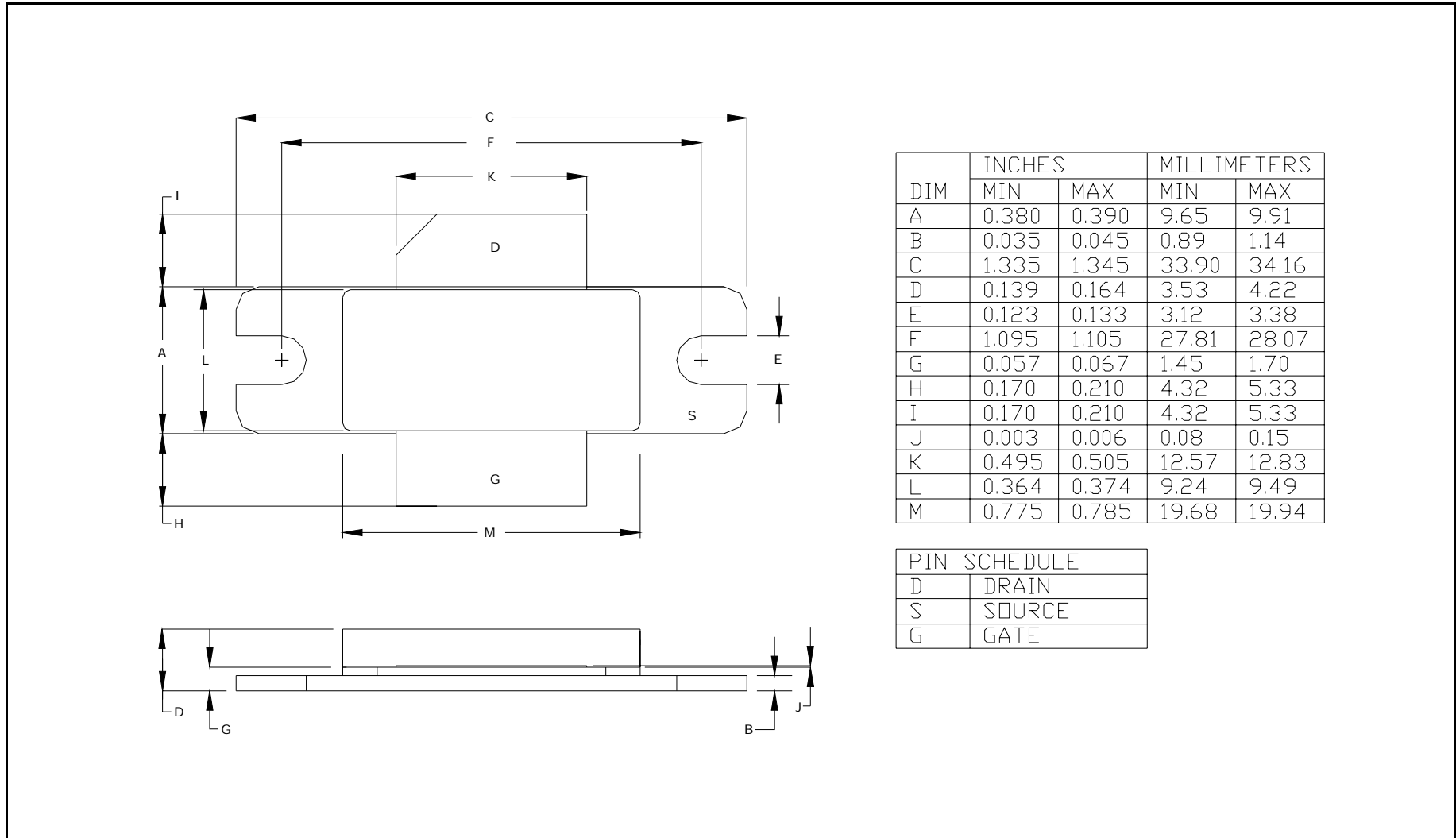
**RF ELECTRICAL CHARACTERISTICS**

| Screen | Parameter  | Symbol | Min  | Max  | Units | Test Conditions   |
|--------|--|--------|------|------|-------|---|
| 100%   | Input Return Loss  | IRL    | -18  | -7   | dB    | $V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$  |
| 100%   | Output Power   | $P_O$  | 140  | 220  | W     | $V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$  |
| 100%   | Drain Efficiency   | $N_D$  | 38   | 60   | %     | $V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$  |
| 100%   | Drain Current  | $I_D$  | 10.0 | 15.0 | A     | $V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$  |
| 100%   | Pulse Amplitude Droop  | D      | -0.5 | +0.5 | dB    | $V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$  |
| 100%   | Delta Insertion Phase  | DIP    | -30  | +30  | DEG   | $V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$  |
| 100%   | 3:1 Load Mismatch Stability  | --     | --   | --   | --    | $V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$<br>Rotate 3:1 output VSWR through 360° phase.<br>No oscillatory or pulse break-up characteristics allowed on detected output pulse. All non-harmonically related signals must be at least -65 dBc. |
| Note 1 | $V1 = 32V; I_{DQ1} = 40mA; PW1 = 300\mu s; DF1 = 10\%, P_{IN1} = 14W.$             |        |      |      |       |   |
| Note 2 | Test Frequencies: $F1 = 2.7\text{ GHz}, F2 = 2.9\text{ GHz}, F3 = 3.1\text{ GHz}.$ |        |      |      |       |   |
| Note 3 | $T_{F1} = 25\pm 5^\circ C =$ Device flange temperature.                            |        |      |      |       |   |
| Note 4 | Screen 'BD' = parameter qualified By Design.                                       |        |      |      |       |   |

**RF TEST FIXTURE IMPEDANCE CHARACTERISTICS**

| Frequency (GHz)      | $Z_{IF}$ ( $\Omega$ )  | $Z_{OF}$ ( $\Omega$ )   |
|----------------------|--|---|
| 2.70                 | 2.35 – j5.64   | 2.47 – j4.83  |
| 2.90                 | 2.31 – j4.47   | 2.59 – j3.82  |
| 3.10                 | 2.27 – j3.53   | 2.71 – j3.20  |
| Impedance Definition |  |  |

**PACKAGE DIMENSIONAL OUTLINE DRAWING**



**RF TEST FIXTURE – ASSEMBLY AND PARTS LIST**

**ASSEMBLY DRAWING**

**PARTS LIST**

PC Board Type: ROGERS RD4350B-03011, 30mil,  
 1/1oz. Copper  
 Aluminum Heatsink: -11  
 Input PC Board Carrier: -3 (1')  
 Output PC Board Carrier: -3 (1')  
 Transistor Copper Carrier: -22  
 RF connector: DS #2052-5636-02  
 Ground: Plated thru vias  
 Banana jack Black -1 place  
 Banana jack Blue - 1 place  
 Banana jack Red -1 place  
 PCB: IPC75 R SQUARE  
 C6,C7,C16: CAP,5.6pF,ATC 600F5R6 EDG MNT..  
 C10,C15: CAP,12pF,ATC 600F120 EDGE MNT..  
 C2,C3,C5,C9: CAP,39PF,ATC600F390J  
 C17: CAP,0.1uF,0805,30V  
 C4,C8: CAP,1uF,0805,25V  
 C1,C18: CAP,1uF,1206,100V  
 C13:CAP,10uF,2220,50V,X7R  
 C19:CAP, 47uF, 50V, ELECTROLYTIC CAP  
 C20:CAP, 100uF, 50V, ELECTROLYTIC CAP  
 C21:CAP, 150uF, 50V, ELECTROLYTIC CAP  
 L1: IND,5N5,1508,  
 L2,L3: IND,FB,120 OHM,0805,5A  
 U1: IC,VREG-ADJ,SOIC-8,LM317LM-ND  
 Q1: PMBT2222  
 R1: RES,1K,0805  
 R2,R3: RES,3.9K,0805  
 R4: RES,2.2K,0805  
 R5: RES,511,0805  
 R8: RES,150,0805  
 R7,R9,R10,R11: RES,5R1,0805  
 R6: RES,VAR,200,4MM,3224W,BDURNS

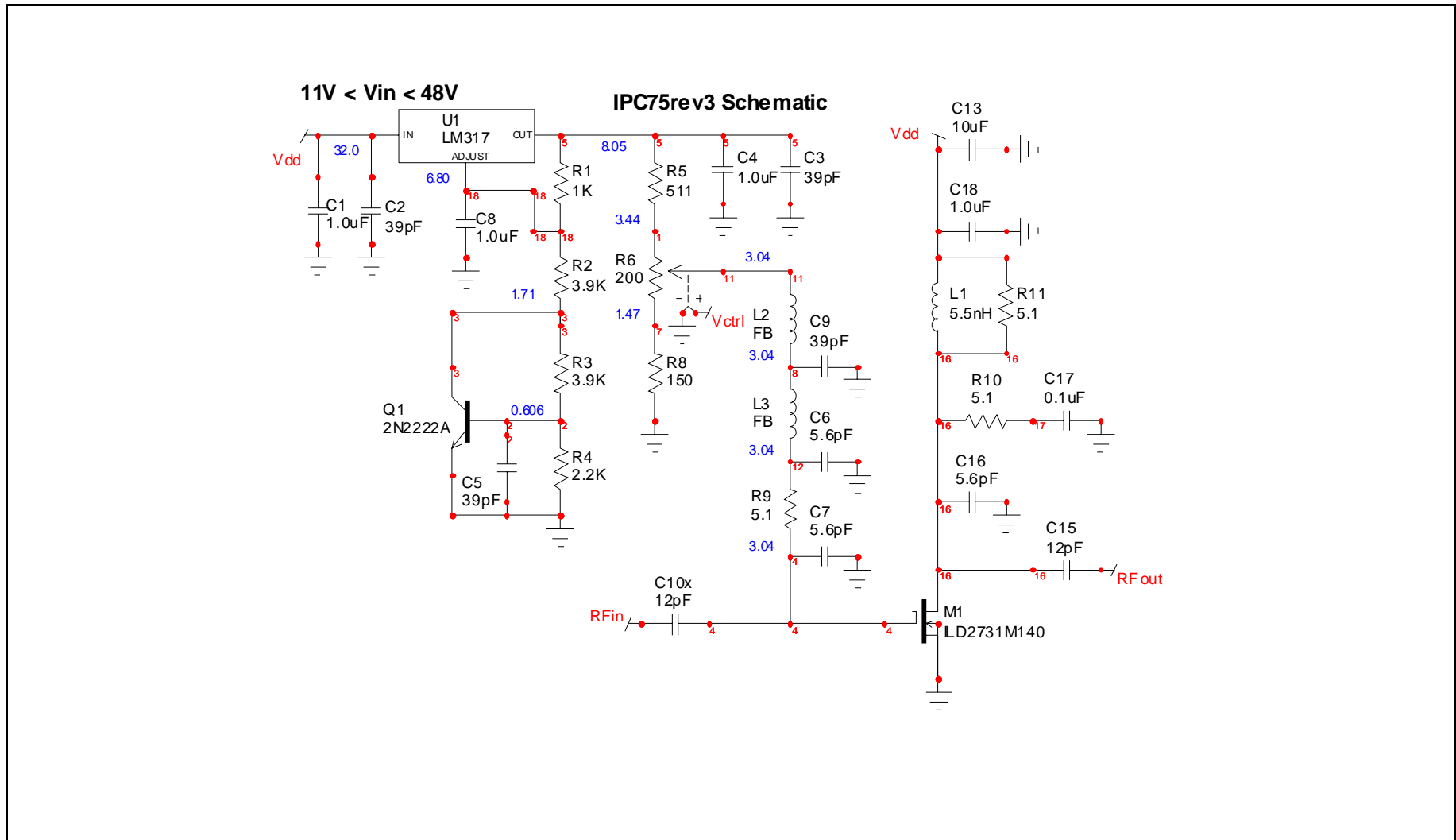
NOTE: IPC75 REV 3

|   |                 |                                      |  |
|---|-----------------|--------------------------------------|--|
| TOLERANCES UNLESS NOTED   |                 | <b>Integra</b><br>TECHNOLOGIES, INC. |  |
| .X ± .1   | X' ± 1'         | ILD2731M140 RF TEST FIXTURE          |  |
| .XX ± .02   | X'X' ± 0'30'    |                                      |  |
| .XXX ± .005   | FRACTION ± 1/32 |                                      |  |
| .XXXX ± .0002   |                 |                                      |  |
| MATERIAL: <b>NOTED</b>  |                 |                                      |  |
| DRAWN: J. BURGER  |                 |                                      |  |
| CHECKED: J. BURGER  |                 | SIZE<br>A                            | DWG NO.<br>ILD2731M140 RF TEST FIXTURE |
| APPROVED: J. DAVIS  |                 | SCALE: 1:1                           | REV<br>A                               |
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**CONTACT FACTORY FOR RF TEST FIXTURE CAD DRAWING WITH CIRCUIT DIMENSIONS**

<L:\Public\Controlled Documents\Controlled Drawings\RF Test Fixture Drawings\ILD2731M140 RF TEST FIXTURE REV A.dwg>

**RF TEST FIXTURE – ELECTRICAL SCHEMATIC**



**DEFINITIONS**

| <b>Data Sheet Status</b>   |   |
|--|---|
| Proposed Specification   | This data sheet contains proposed specifications.                                   |
| Preliminary Specification  | This data sheet contains specifications based on preliminary measurements and data. |
| Product Specification  | This data sheet contains final product specifications.                              |
| <b>Maximum Ratings</b>   |   |
| Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability. |   |

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