

Part Number: ILD3135M180

S-Band Radar Transistor

Part number ILD3135M180 is designed for S-Band radar applications operating over the 3.1 – 3.5 GHz instantaneous frequency band. Under 300us / 10% pulsing conditions it supplies a minimum of 180 watts of peak output power with 11dB gain typically. Specified operation is with Class AB bias. The single-ended broadband test fixture includes a temperature compensated bias network. All devices are 100% screened for large signal RF parameters in a fixed tuned broadband matching circuit / test fixture. The use of external tuners is not allowed during screening. This device is rated for a peak output power level of $P_{PEAK} = 180W$ @ 10% duty factor. This corresponds to an average power $P_{AVG} = 18W$.



TYPICAL DATA TYPICAL DATA TYPICAL DATA TYPICAL DATA

Freq (GHz)	PW (uS)	Duty (%)	Pout (W)	IRL (dB)	Gp (dB)	Id (A)	Nd (%)	Droop (dB)	VSWR-S (3:1)
3.1	300	10	180	-17	11.8	13.7	41	-0.1	Pass
3.3	300	10	180	-15	12.3	14.1	40	-0.1	Pass
3.5	300	10	180	-12	11.8	15.2	37	-0.1	Pass

VDD=32V, IDQ=60mA

Integra

TECHNOLOGIES, INC.

Silicon LDMOS FET

- High Power Gain
- Excellent thermal stability
- Gold Metal

Gold Metal System

- Complete Gold System
- LDMOS with Gold Metal
- Gold Bond Wires
- Gold Package Metal
- Maximum Reliability

Class AB Operation

- Specified with AB bias

Internal Impedance Matching

- Ease of Use
- Ultra Low Loss Design

BeO Free Package

- Metal Based
- Epoxy Seal

High Power RF Test / Fixture

- Single-ended
- Broadband
- Matched to 50 Ω (ohms)
- Temperature Compensated Bias
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning required

MAXIMUM RATINGS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Drain-Source Voltage	V_{DS}	--	65	V	--
BD	Gate-Source Voltage	V_{GS}	-0.5	12	V	--
BD	Storage Temperature Range	T_{STG}	-55	+150	°C	--
BD	Operating Junction Temperature Range	T_J	-55	+200	°C	--
BD	CW Operation	--	--	--	--	Not recommended for CW operation.
Note	Screen 'BD' = parameter qualified By Design.					

THERMAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	0.13	°C/W	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{OUT}=180W, N_D=33\%$
Note	Screen 'BD' = parameter qualified By Design.					

PROCESSING SPECIFICATIONS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071.6, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					



DC ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Drain-Source Breakdown Voltage	BV_{DSS}	65	--	V	$I_{DS}=10mA, V_{GS}=0V, T_F=25\pm5^\circ C$
100%	Drain Leakage Current	I_{DSS}	--	10	uA	$V_{DS}=32V, V_{GS}=0V, T_F=25\pm5^\circ C$
100%	Operating Gate Voltage	V_{GS}	2.5	4.0	V	$V_{DS}=5V, I_D=0.10A, T_F=25\pm5^\circ C$
100%	Gate Leakage Current	I_{GSS}	--	1.0	uA	$V_{GS}=10V, V_{DS}=0V, T_F=25\pm5^\circ C$

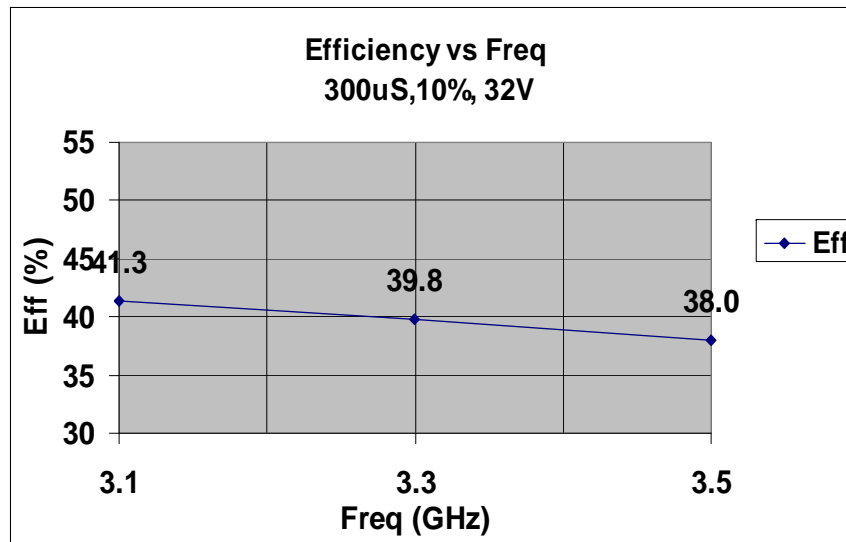
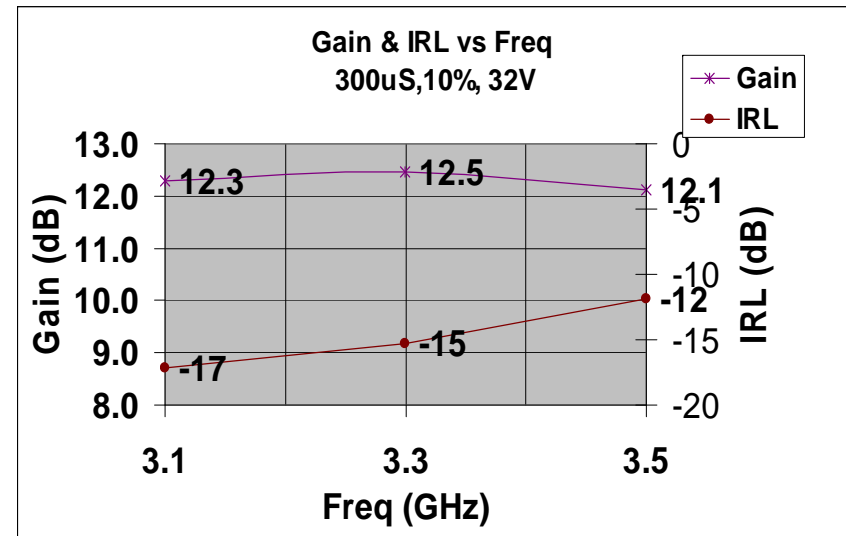
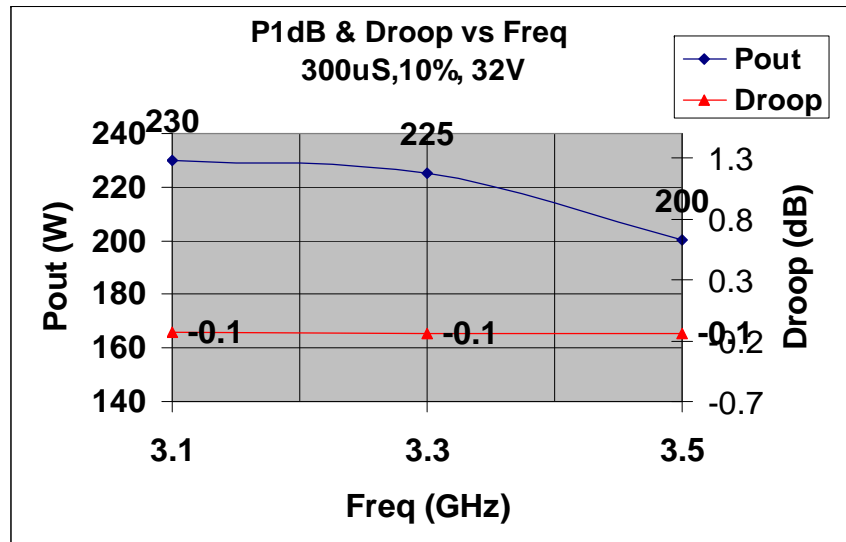
RF ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	IRL	-18	-7	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{OUT}=P_{OUT1}, F=F1, F2, F3.$
100%	Pin	Pin	9.0	20.3	W	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{OUT}=P_{OUT1}, F=F1, F2, F3.$
100%	Power Gain	Gp	9.5	13	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{OUT}=P_{OUT1}, F=F1, F2, F3.$
100%	Drain Efficiency	N_D	33	60	%	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{OUT}=P_{OUT1}, F=F1, F2, F3.$
100%	Pulse Amplitude Droop	D	-0.5	+0.5	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{OUT}=P_{OUT1}, F=F1, F2, F3.$
100%	3:1 Load Mismatch Stability	VSWR-S	Pass	--	P/F	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{OUT}=P_{OUT1}, F=F1, F2, F3.$ Rotate 3:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse. All non-harmonically related signals must be at least -65 dBc.
100%	Gain Flatness	GF	0	1.25	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{OUT}=P_{OUT1}, F=F1, F2, F3.$
100%	Delta Insertion Phase	DIP	-30	+30	DEG	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{OUT}=P_{OUT1}, F=F3.$ Measure at 50% of pulse ontime. Bin per marking table.
Note 1	V1 = 32V; I_{DQ1} = 60mA; PW1 = 300us; DF1 = 10%, P_{OUT1} = 180W Peak, 18W Ave					
Note 2	Test Frequencies: F1 = 3.1 GHz, F2 = 3.3 GHz, F3 = 3.5 GHz.					
Note 3	T_{F1} = 25±5°C = Device flange temperature.					
Note 4	Screen 'BD' = parameter qualified By Design.					

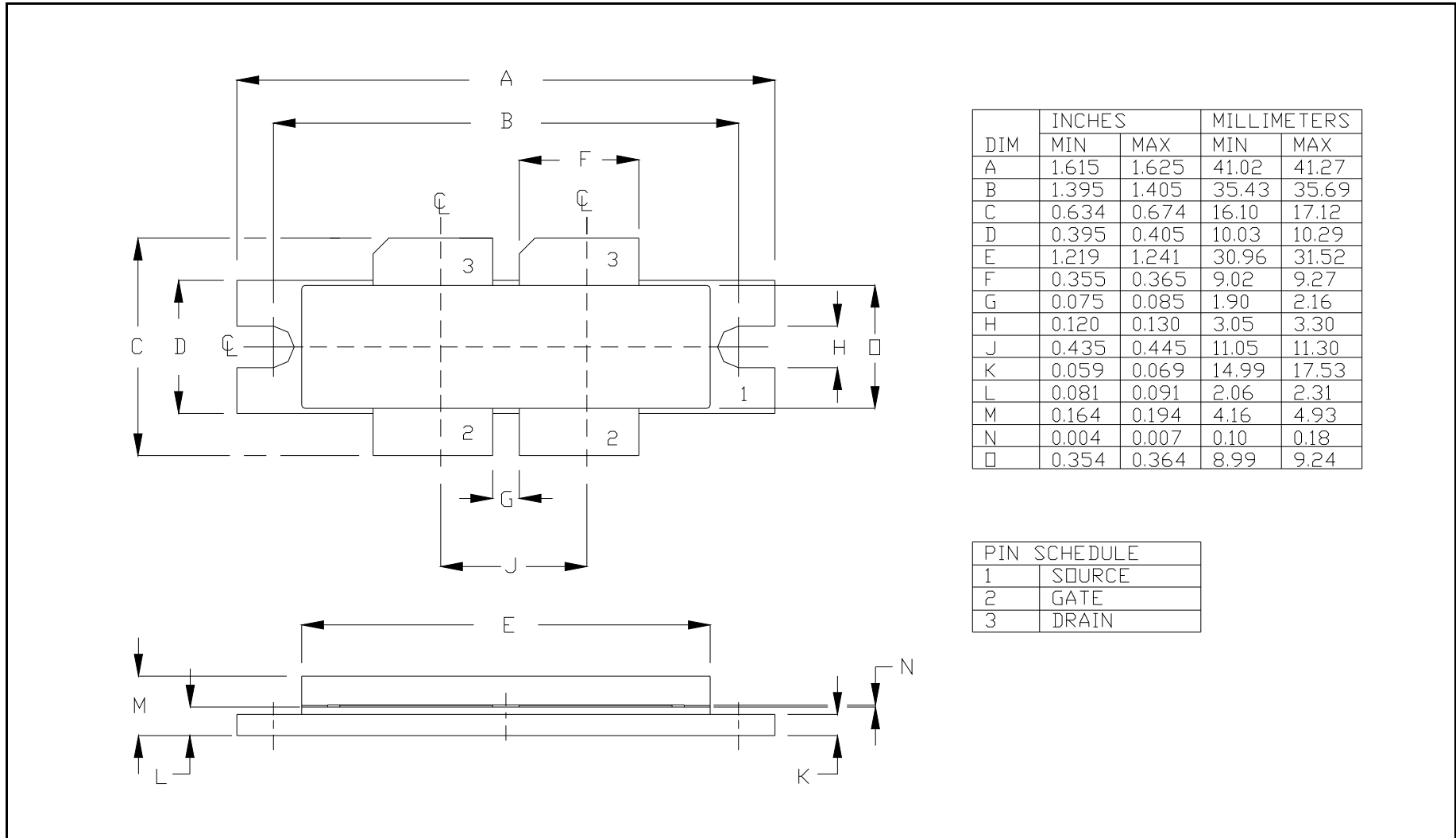
RF TEST FIXTURE IMPEDANCE CHARACTERISTICS

Frequency (GHz)	Z_{IF} (Ω)	Z_{OF} (Ω)
3.10	2.2 - j1.4	2.3 + j1.7
3.30	2.0 - j0.3	2.1 + j2.4
3.50	1.8 + j0.7	1.8 + j3.1
Impedance Definition		

PERFORMANCE GRAPHS (Pout=180W except as noted)



PACKAGE DIMENSIONAL OUTLINE DRAWING



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.615	1.625	41.02	41.27
B	1.395	1.405	35.43	35.69
C	0.634	0.674	16.10	17.12
D	0.395	0.405	10.03	10.29
E	1.219	1.241	30.96	31.52
F	0.355	0.365	9.02	9.27
G	0.075	0.085	1.90	2.16
H	0.120	0.130	3.05	3.30
J	0.435	0.445	11.05	11.30
K	0.059	0.069	14.99	17.53
L	0.081	0.091	2.06	2.31
M	0.164	0.194	4.16	4.93
N	0.004	0.007	0.10	0.18
□	0.354	0.364	8.99	9.24

PIN SCHEDULE	
1	SOURCE
2	GATE
3	DRAIN

RF TEST FIXTURE – ASSEMBLY AND PARTS LIST

ASSEMBLY DRAWING

PARTS LIST

PC Board Type: ROGERS RD4350B-03011, 30mil,
1/1oz. Copper
Aluminum Heatsink: RPK005 ILD501 HEATSINK
Input PC Board Carrier: -3 (1)
Output PC Board Carrier: -3 (1)
Transistor Copper Carrier: RPK-003B-003
RF connector: DS #2052-5636-02
Ground Plated thru vias (DR GND STRAPS PER
BELLOW)
Banana Jack Black -1 places
Banana Jack Blue - 1 place
Banana Jack Red -1 places
C7,C16,C19: CAP,5.6pF,ATC 600F5R6 EDG MNT.
C10,C15: CAP,12pF,ATC 600F120 EDGE MNT.
C2,C3,C5,C9: CAP,399F,ATC600F390J
C1,C4,C6,C17,C20: CAP,0.1UF,0805,50V
C8,C18,C21: CAP,1uF,1206,100V
C13,C22: CAP,10uF,2220,50V,X7R
C23: CAP, 47UF, 50V, ELECTROLYTIC CAP
C24: CAP, 100UF, 50V, ELECTROLYTIC CAP
C25: CAP, 150UF, 50V, ELECTROLYTIC CAP
L1,L4: IND,5N5,1508,
L2,L3: IND,FB,120 IHM,0805,5A
U1: IC,VREG-ADJ,SDIC-8,M317LM-ND
Q1: PMBT2222
R1: RES,1K,0805
R2,R3: RES,3.9K,0805
R4: RES,2.2K,0805
R5: RES,4.7K,0805
R6: RES,1.5K,0805
R7,R9,R10,R11,R12,R13: RES,5R1,0805
R6: RES,VAR,2K,4MM,3224W,BURNS

NOTES
1)GSI-GS23: GROUND STRAP, FILD AS SHOWN. GS
CAN BE USED INSTEAD OF PLATED VIAS.
2)SHOULDER WASHER KEYSTONE #3229 DN
RED/BLUE JACKS. NO WASHER NEEDED DN BLACK.
3)JACKS SCREWED IN WITH 2-56 SCREWS

TOLERANCES UNLESS NOTED		Integra TECHNOLOGIES, INC.	
.X ± .1	X' ± 1"	ILD3135M180 RF TEST FIXTURE	
.XX ± .02	X'X' ± 0'30"		
.XXX ± .005	FRACTION ± 1/32		
.XXXX ± .0002			
MATERIAL: NOTED		REV C	
DRAWN: R KESHISHIAN			
CHECKED: J BURGER			
APPROVED: J. DAVIS		SIZE A	DWG NO. ILD3135M180 RF TEST FIXTURE
		SCALE: 1:1	SHEET: 1 of 2

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CONTACT FACTORY FOR RF TEST FIXTURE CAD DRAWING WITH CIRCUIT DIMENSION
<L:\Public\Controlled Documents\Controlled Drawings\RF Test Fixture Drawings\ILD3135M180 RF TEST FIXTURE REV C.dwg>

DEFINITIONS

Data Sheet Status	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
Maximum Ratings	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

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