Part Number: ILT2731M30

Integra
TECHNOLOGIES, INC.

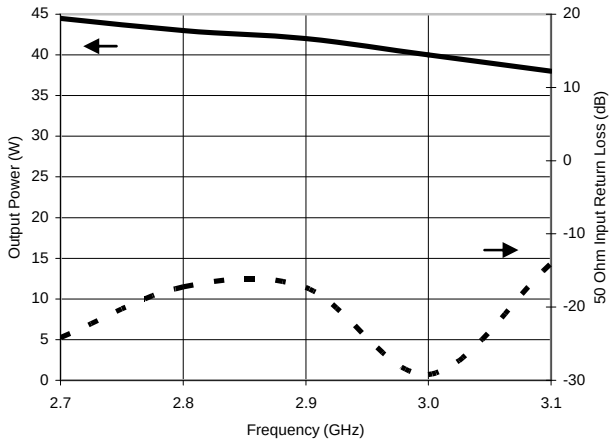
S-Band Radar 50 Ω Transistor

Part number ILT2731M30 is a high power transistor which is internally matched to 50 ohms. It is designed for S-Band radar systems and operates over the instantaneous bandwidth of 2.7-3.1 GHz. It utilizes gold metal LDMOS transistor technology operating in common source configuration. Production RF performance screening is performed at the 100% level while operating under class AB bias (IDQ = 10mA) with a 300us pulse width at 10% duty. The device is operable under a wide range of biasing and pulsing conditions. This device is rated for a peak output power level of PPEAK = 30W @ 10% duty factor. This corresponds to an average power PAVG = 3W.

Operate any power level from due to linear transfer curve

TYPICAL OUTPUT POWER VERSUS FREQUENCY PERFORMANCE

ILT2731M30 : Pin = 2W /3100us / 10% / 32V / Idq=10mA



50 Ohm Matched
- Requires no external impedance matching circuitry

Silicon LDMOS Transistor
- Gold Metal

Class AB Operation
- Operable under a wide range of bias conditions

Common Source Configuration
- Chip internal Source grounding

Gold Metal System
- Complete Gold System Including Bond-wires
- Maximum Reliability

Be0 Free Package
- Metal Based
- Epoxy seal

RF High Power Test
- 100% Device RF High Power Screening

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MAXIMUM RATINGS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Drain-Source Voltage	V_{DS}	--	65	V	--
BD	Gate-Source Voltage	V_{GS}	-0.5	12	V	--
BD	Storage Temperature Range	T_{STG}	-55	+150	°C	--
BD	Operating Junction Temperature Range	T_J	-55	+200	°C	--
BD	CW Operation	--	--	--	--	Not rated for CW operation.
Note	Screen 'BD' = parameter qualified By Design.					

THERMAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	0.38	°C/W	V_{DD}=V1, I_{DQ}=I_{DQ}1, PW=PW1, DF=DF1, T_F=TF1, P_{IN}=P_{IN1}, F=F3.
Note	Screen 'BD' = parameter qualified By Design.					

PROCESSING SPECIFICATIONS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

DC ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Drain-Source Breakdown Voltage	BV_{DSS}	65	--	V	I_{DS} = 10mA, V_{GS} = 0V, T_F = 25±5°C.
100%	Drain Leakage Current	I_{DSS}	--	2.0	µA	V_{DS} = 32V, V_{GS} = 0V, T_F = 25±5°C.
100%	Operating Gate Voltage	V_{GS}	1.5	4.0	V	V_{DS} = 5V, I_D = 0.1A, T_F = 25±5°C.
BD	Gate Leakage Current	I_{GSS}	--	2.0	µA	V_{GS} = 10V, V_{DS} = 0V, T_F = 25±5°C.

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RF ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	IRL	-18	-10	dB	V_{DD}=V1, I_{DQ}=I_{DQ}1, PW=PW1, DF=DF1, T_F=TF1, P_{IN}= P_{IN1}, P_{IN2}, P_{IN3}, F=F1, F2, F3.
100%	Power Gain	G_P	11.0	15.0	dB	V_{DD}=V1, I_{DQ}=I_{DQ}1, PW=PW1, DF=DF1, T_F=TF1, P_{IN}= P_{IN1}, P_{IN2}, P_{IN3}, F=F1, F2, F3.
100%	Power Gain Flatness versus Frequency	GF	0.0	1.3	dB	V_{DD}=V1, I_{DQ}=I_{DQ}1, PW=PW1, DF=DF1, T_F=TF1, P_{IN}= P_{IN1}, P_{IN2}, P_{IN3}, F=F1, F2, F3.
100%	Drain Current - Peak	I_D	1.00	4.00	A	V_{DD}=V1, I_{DQ}=I_{DQ}1, PW=PW1, DF=DF1, T_F=TF1, P_{IN}= P_{IN1}, P_{IN2}, P_{IN3}, F=F1, F2, F3.
100%	Pulse Amplitude Droop	D	-0.50	+0.20	dB	V_{DD}=V1, I_{DQ}=I_{DQ}1, PW=PW1, DF=DF1, T_F=TF1, P_{IN}= P_{IN1}, P_{IN2}, P_{IN3}, F=F1, F2, F3.
100%	Stability into 3:1 VSWR	VSWR-S	--	--	--	V_{DD}=V1, I_{DQ}=I_{DQ}1, PW=PW1, DF=DF1, T_F=TF1, P_{IN}= P_{IN1}, P_{IN2}, P_{IN3}, F=F1, F2, F3. Rotate 3:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse. All non-harmonically related signals must be at least –65 dBc.

Note 1	V1 = 32V; I_{DQ}1 = 10mA; PW1 = 300µs; DF1 = 10%
Note 2	Input Power Test Levels: P_{IN0} = P_{IN1} = P_{IN2} = P_{IN3} = 2.0W
Note 3	Test Frequencies: F1 = 2.7 GHz, F2 = 2.9 GHz, F3 = 3.1 GHz
Note 4	T_F = 25±5°C = Device Flange Temperature

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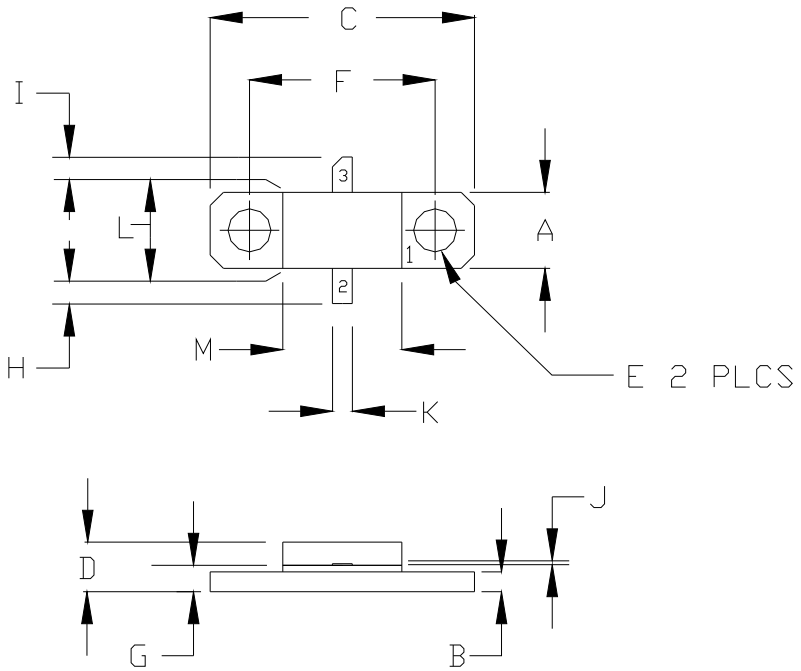
PACKAGE DIMENSIONAL OUTLINE DRAWING



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.225	0.235	5.71	5.96
B	0.055	0.065	1.40	1.65
C	0.795	0.805	20.19	20.44
D	0.140	0.160	3.55	4.06
E	0.125	0.135	3.18	3.43
F	0.557	0.567	14.14	14.40
G	0.077	0.087	1.95	2.20
H	0.093	0.107	2.36	2.72
I	0.093	0.107	2.36	2.72
J	0.004	0.006	0.10	0.15
K	0.055	0.065	1.40	1.65
L	0.225	0.235	5.71	5.96
M	0.355	0.365	9.01	9.27

PIN SCHEDULE	
1	SOURCE
2	GATE
3	DRAIN

NOTES:

LID: SEE BOM

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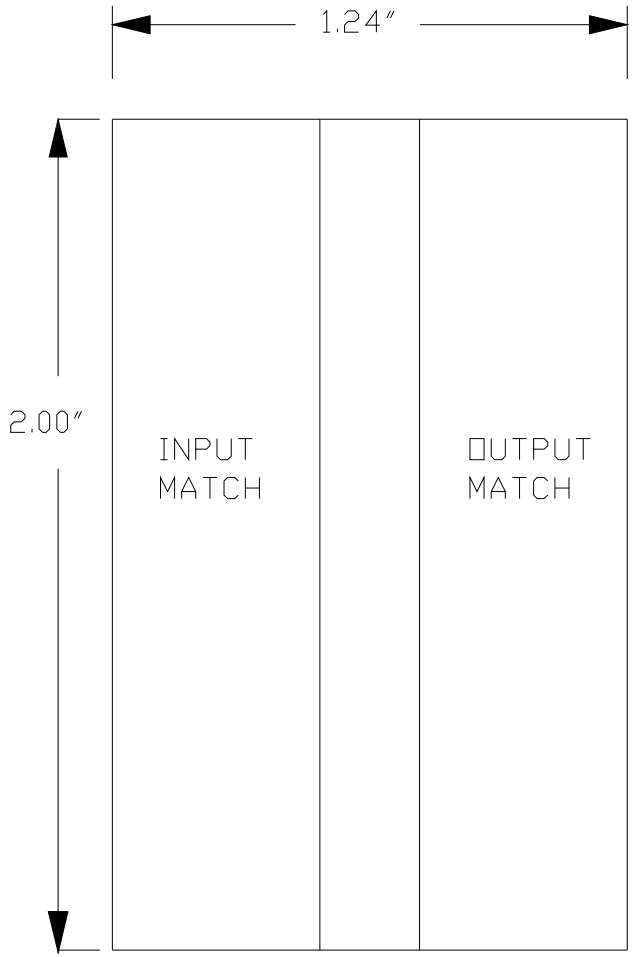
RF TEST FIXTURE



CONTACT FACTORY FOR RF TEST FIXTURE CAD DRAWING WITH CIRCUIT DIMENSIONS

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DEFINITIONS

Data Sheet Status	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.

Maximum Ratings
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only. Operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.

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