Mixed-Mode Class E-F^{-1} High Efficiency GaN Power Amplifier for P-Band Space Applications

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Abstract — A GaN based high efficiency, high power amplifier in P-band for space borne radar applications is demonstrated. It uses a single chip transistor that achieves 250W output power with greater than 80% drain efficiency from 420MHz to 450MHz, using a pulsed waveform with 10% duty cycle. The circuit topology is based on a combination of class E and inverse class F harmonic tuning.

Index Terms — amplifier, class E, GaN, inverse class F, P-band, space, switch-mode, radar.

I. Introduction

Several space amplifier applications are adopting GaN technology due to the superior physical properties that this material offers. In reference [1] a 120W GaN amplifier module is reported with 60% efficiency for L-band SweepSAR radar systems. In reference [2] a comparison is made of class E, F and inverse F amplifiers in L-band (2 GHz) to determine the best performance achievable with a 10W GaN transistor targeted for satellite radio navigation (Galileo). In reference [3] the typical performance goals of output power, bandwidth and overall efficiency are outlined for a T/R module in L-band for future space needs.

Besides L-band, several space applications exist in P-band requiring high power and efficiency capabilities which have attracted significant development using GaN against other technologies: VDMOS/LDMOS are not radiation-hardened; GaAs uses low voltage, which adds high losses in power supply; bipolar has low gain; so that opens the door to GaN. Also, GaN has lowest output pF/W figure of merit which is an essential requirement for high efficiency switched amplifiers. For instance, Synthetic Aperture Radar (SAR) imaging of subsurface features for Mars, as suggested in reference [4], or other non-terrestrial objects, or the terrestrial surface itself, all benefit from power amplifiers based on GaN technology. Here, a high power amplifier in P-band would allow deeper ground penetration and subsurface imaging. Future interplanetary missions using Multi-Mission Subsurface Imaging Radar (MMSIR) technology would also benefit from a GaN based amplifier. An airborne test bed system for Biomass estimation (Airmoss) is in operation using P-Band SAR, which is the precursor to future space instruments [5]. With space operated radar instrumentation, it becomes mandatory matching the high output power requirements of an amplifier with high efficiency to keep power supply requirements and weight manageable, while at the same time improving packaging and printed circuit board materials and techniques [6].

The purpose of the research work presented in this paper is to demonstrate a 250W GaN single transistor building block aimed at high power amplifier for P-Band radar applications such as space exploration and earth remote sensing, with efficiency targets above 80%. The power amplifier utilizes GaN HEMT device technology; we show results with GaN chips optimized to operate at 75V and 100V supply voltage, with impedance matching circuits that include harmonic tuning to optimize efficiency. The ultimate goal is to create an amplifier module with greater than 80% efficiency from 420MHz to 450MHz, using a pulsed waveform with 10% duty cycle. The objective has been achieved by implementing an impedance matching scheme that results in a combination of class E and inverse class F topology.

II. High Voltage GaN HEMT Technology

Our research work uses a GaN transistor built with a single chip to achieve a target of 250W minimum output power and 80% drain efficiency. Two different die configurations have been developed, with the following characteristics:

1) a 21mm die operating at 75V with 250W output power, 22dB gain and drain efficiency in excess of 80%;
2) a 15mm die operating at 100V with 250W output power, 25dB gain and drain efficiency in excess of 75%.

The chip operating at 75V has a breakdown voltage in excess of 200V, whereas the die designed to operate at 100V has a breakdown voltage exceeding 300V. Both chips versions are available with 0.5µm and 1µm gate length, whereas the main difference between the 75V and the 100V GaN HEMT devices is the length of the gate-drain extension (drift region) and the relative source connected field plate. The two different layout topologies were selected to address not only potential differences in thermal resistance and junction temperature, but also F/2 or harmonic spurious signals under mismatch and stability. The different die architectures also translate into different combining properties when building a transistor with two or more chips inside one package, targeting a 500W or higher output power level.

The test device uses an input LC resonance to increase the input gate impedance, and the drain is bonded directly to the transistor output lead to allow for fundamental and harmonic

tuning outside the transistor package. The test environment used test fixtures with fixed tuned load impedances for all measurement frequencies with no external tuners. Separate test fixtures were created for each operating voltage and corresponding load line impedance. A picture of the package and internal device assembly is shown in Fig. 1.

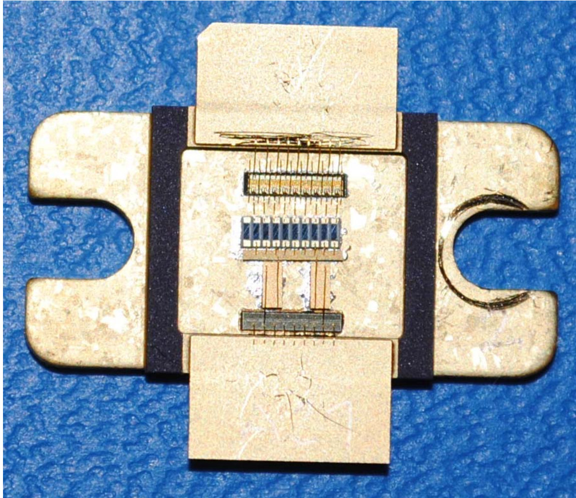

Fig. 1. Package and internal assembly of GaN transistor.

III. HARMONIC TUNED CIRCUIT TECHNIQUES

To determine the quality of each test fixture load match, the measured values at the package reference plane are de-embedded and then compared to optimum fundamental and harmonic load impedances for Inverse Class F or Class E operation. The derivation of the model uses the combination of a calculation for Rds and estimate of Cds (die output and package lead capacitances) by overlapping the model impedance to the load pull measured results. The de-embedding process is based on a model of the die and package as shown in Fig. 2.

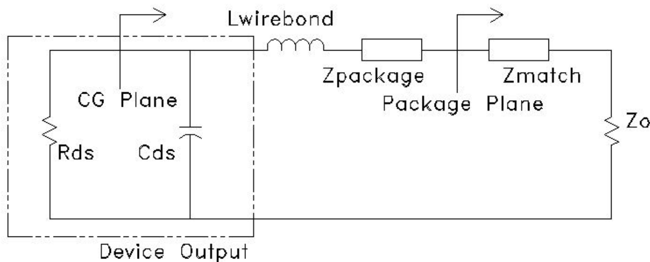

Fig. 2. Device Output Model and Current Generator Load Impedance.

To approximate the real impedance at the current generator, we have used calculations based on inverse Class F operation from Grebennikov [7], where Rds (class F^{-1}) = $\pi/2$ Rds (class B), and Rds (class B) = Vdd^2 / (2·Pout). We get 17.7 ohms at 75V and 31.4 ohms at 100V, using 250W output power.

Starting with the calculated value for Rds, the value for Cds was adjusted to match the packaged device model to the load pull result. Cds is 10.5pF and 7.5pF at 75V and 100V, respectively. Series inductance is 0.1nH for all cases. The data are then compared to the optimum load impedances for an Inverse Class F and Class E amplifiers as described in [7] and [8]. A similar approach is discussed in reference [9]. The data are summarized in Table 1.

TABLE1
Normalized Optimum Load Impedances for Inverse Class F and Class E

	Class E	**Class F^{-1}**	**75V TF**	**100V TF**
F_0	1+j0.725	1	1+j0.15	1+j0.19
2 F_0	-j1.785	∞	0.11-j1.05	0.06-j0.51
3 F_0	-j1.19	0	0.01-j0.42	0.03-j0.19

The results highlight the uncertainty for the class of operation, as the fundamental and harmonic impedances in this case do not define the amplifier class of operation. The impedance results define an amplifier class that is a combination of Inverse Class F and Class E operation. A picture of the test fixture for the 75V device is shown in Fig 3.

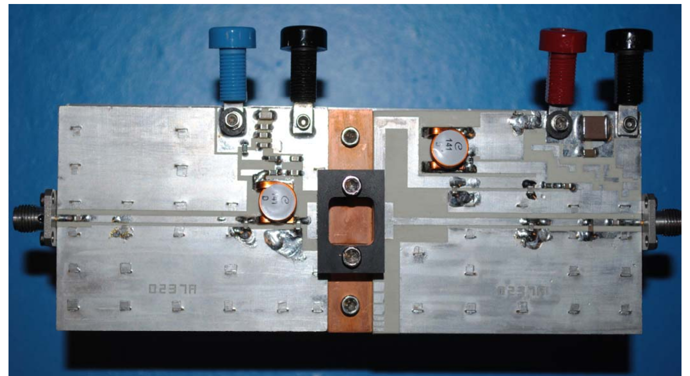

Fig. 3. Picture of the test fixture for the 75V GaN device. Input and output matching consists mainly of 50 ohm transmission lines with shunt capacitors to tune first, second and third harmonics.

IV. RF RESULTS

Single GaN die evaluations were done to select the best solution for achieving greater than 80% drain efficiency and 250W output power. Data was collected on available saturated output power, drain efficiency, power gain, pulse droop, and stability under 2:1 VSWR mismatch. RF data measured on sample devices is presented in Fig. 4, 5, 6, 7 and 8. The device performance is measured at saturated power, which is defined

at the point where the die is gain compressed enough to cause gate current to flow. This saturated power level is approximately 4dB to 5dB gain compression from a low output power reference, typically >10dB drive power below the saturation point.

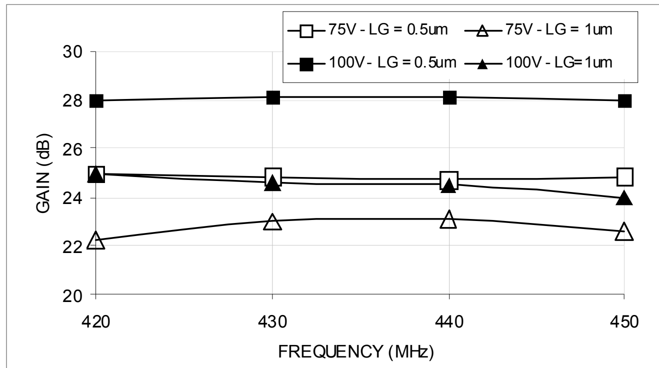

Fig. 4. Power Gain Performance at 250W – Die Comparison

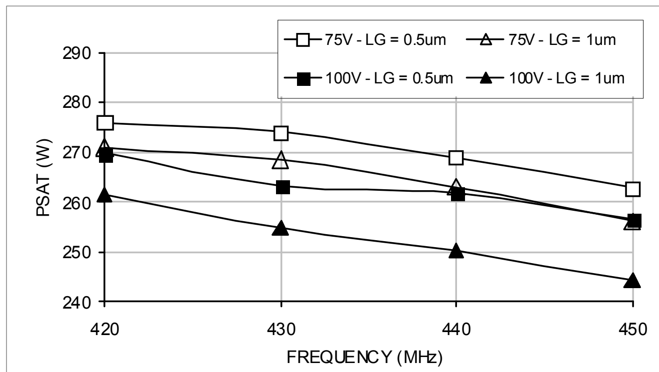

Fig. 5. Saturated Output Power Performance – Die Comparison

It can be seen in Fig. 4 that increasing the gate length from 0.5µm to 1.0µm reduces gain by approximately 3dB, whereas the 100V chip design has almost 3dB more gain than the 75V die design. Comparing the test fixture normalized harmonic impedances for the 75V and 100V devices to the efficiency results in Fig. 6, it can be seen that there is a correlation to the efficiency results and test fixture harmonic loads.

The saturated output power across the frequency band 420-450MHz is about the same for the four devices, as seen in Fig. 5, although the power density is different due to the 15mm versus 21mm gate periphery in the two designs. On the contrary, efficiency is higher for the 75V devices compared to the 100V samples, as seen in Fig. 6. The pulse droop during a 300us pulse is shown in Fig. 7 for all four devices. The pulse droop is measured by sampling the pulse at 10% time point of the pulse and at the 90% time point of the pulse. Pulse droop results correlate with drain efficiency, and it is lower where the efficiency is higher.

The lower efficiency observed for the 100V die types was due to the circuit topology used. The simple topology of the test circuit made it difficult to achieve proper impedance ratios between the fundamental and harmonic frequencies as the voltage is increased. Pulse droop tends to be higher with lower efficiency and higher power density (Watts per mm of gate periphery, which is higher on 100V chip design).

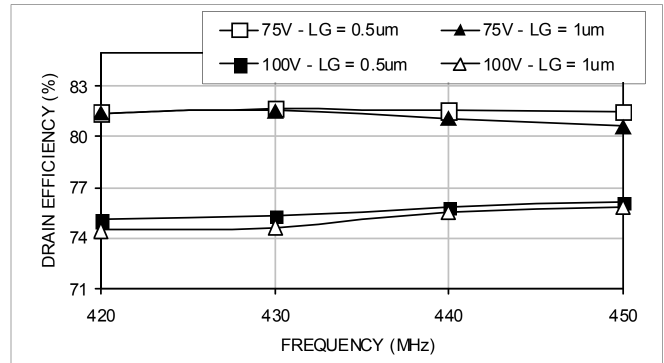

Fig. 6. Drain Efficiency Performance – Die Comparison

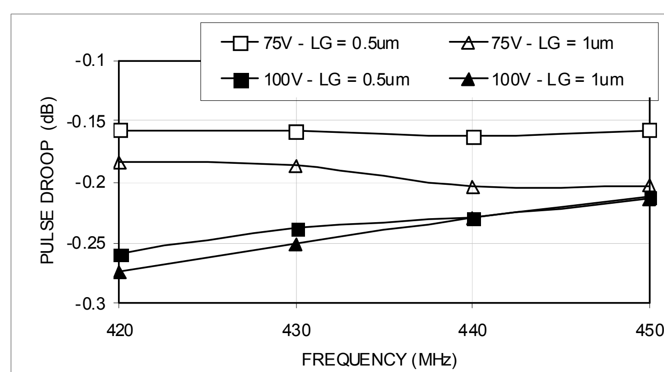

Fig. 7. Pulse Droop Performance – Die Comparison

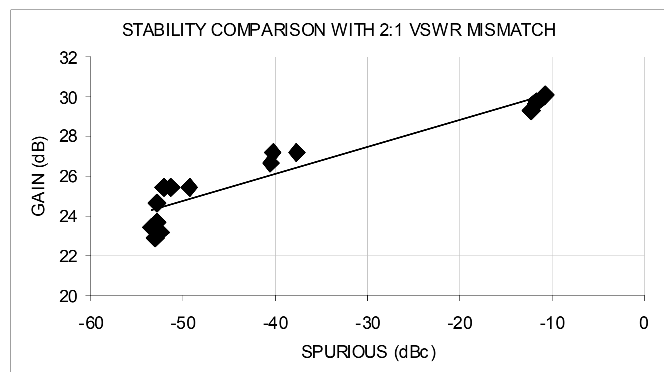

Fig. 8. Stability vs. Spurious Performance – Die Comparison

Very high RF gain at low frequencies can cause instabilities and power sharing issues, which can result in spurious emissions from the amplifier and possible device failures. To understand the possible implications of the very high gain observed by the test samples, each device was subjected to a

2:1 VSWR mismatch at the output with all phase angles. Fig. 8 shows a correlation between observed spurious under a 2:1 mismatch and the gain of the device at rated power. Although all chip types show the capability to achieve 250W and high efficiency, our results indicate that the best die selection moving forward for a multi-chip device design will be the 75V, 1µm gate length, 21mm gate periphery die. This device has the required saturated output power capability and the lowest gain to help mitigate low frequency instability issues.

The thermal resistance of the 15mm 100V devices has been calculated, as described in reference [10], to be 0.36 °C/W for the bare die, whereas for the 21mm 75V devices it is 0.31 °C/W. We have used a value of 300 W/m-°K for the thermal conductivity of the SiC substrate. The thermal resistance component for the package CPC flange is ~0.1 °C/W in both cases. Therefore the total thermal resistance of the 100V devices tested is 0.46 °C/W, and for the 75V devices it is 0.41 °C/W. At 420MHz, the 100V sample with 0.5µm gate length has 270W output power and 75% drain efficiency; therefore the DC power is 360W, and the dissipated power is 360W-270W=90W. For a base-plate temperature of 35 °C under forced air cooling, the calculated peak channel temperature is 76.4 °C which is very good from a reliability standpoint. A similar calculation at 420MHz for the 75V 1.0µm gate length device has 270W saturated output power and 81% drain efficiency; therefore the DC power is 333W, and the dissipated power is 333W-270W=63W. For a base-plate temperature of 35 °C under forced air cooling, the calculated peak channel temperature is now 60.8 °C which is also very good from a reliability standpoint. A more accurate analysis of the junction temperature has to account for the 300us pulse length with a 10% duty cycle. Time-domain simulations of the junction temperature under the specified pulse conditions have been carried out and the results are shown in Fig. 9.

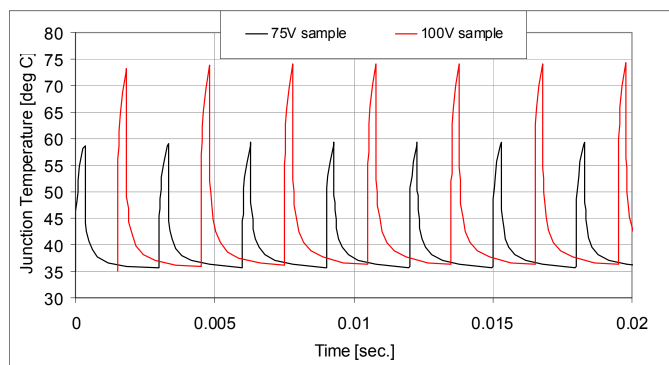

Fig. 9. Junction temperature versus time for the 75V and 100V samples with 63W and 90W dissipated power, respectively. The data for the 100V chip are shifted by 1.5ms to facilitate the viewing of the junction temperature peaks.

Junction temperature on the 75V device barely reaches 60 °C, whereas on the 100V device it approaches 75°C, in good agreement with the projections made above. Gate length has only minor effect on the junction temperature. Notice how the more efficient 75V devices operate at lower peak junction temperatures compared to the 100V devices, which translates into better reliability.

V. Conclusion

Several single GaN chip transistors have been evaluated for a 250W output power, 80% efficiency amplifier at P-band for radar applications in space exploration and earth remote sensing. The results are obtained with a circuit topology where the measured impedances are typical of a combination between class E and inverse class F power amplification. It has been demonstrated stable operation at 75V and 100V bias of a 250W power amplifier with greater than 80% efficiency and estimated junction temperature well below the 150 °C level needed for high reliability operation.

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References

[1] T. Thrivikraman, S. Horst, D. Price, J. Hoffman and L. Veilleux, “A Compact Two-stage 120W GaN High Power Amplifier for SweepSAR Radar Systems,” *2014 IEEE Aerospace Conference*, March 2014.

[2] A. Ramadan, A. Martin, D. Sardin, T. Reveyrand, J-M. Nebus, P. Bouyesse, L. Lapierre, J. F. Villemazet and S. Forestier, “Study and Design of High Efficiency Switch Mode GaN Power Amplifiers at L-band Frequency,” *Advances in Computational Tools for Engineering Applications*, 2009. ACTEA '09.

[3] W. N. Edelstein, C. Andricos, S. Madsen, F. Wang and D. B. Rutledge, “Current Status of the High-Efficiency L-band Transmit/Receive Module Development for SAR System”, Earth Science Technology Conference, June 2003.

[4] K. K. Williams and R. Greely, “Radar Imaging of Subsurface Geology through Sand: Analysis of Penetration Depth Variables With Implications For MARS Exploration”, *Lunar and Planetary Science XXXI*, p. 1023

[5] http://airmoss.jpl.nasa.gov

[6] J. P. Hoffman, L. D. Castillo, J. Miller, M. Jenabi and G. Birur, “Advanced packaging materials and techniques for high power T/R module”, *Earth Science Technology Forum*, 2011.

[7] Andrei Grebennikov, Nathan Sokal, “Switch Mode RF Power Amplifiers,” Elsevier, Burlington MA USA, pg. 160, 2007.

[8] F. Raab, “Class-E. Class-C, and Class F Power Amplifiers Based upon a Finite Number of Harmonics,” *IEEE Transactions on Microwave Theory and Techniques*, Vol. 49, No. 9, August 2001, pp 1462-1468.

[9] James Custer, Gabriele Formicone, ‘High Efficiency Switch Mode GaN-based Power Amplifiers for P-Band Aerospace Applications,’ *2014 IEEE Aerospace Conference*, March 2014.

[10] John L. B. Walker, “High-Power GaAs FET Amplifiers,” Arthech House., 1993, p.234.

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