

S-Band Radar Transistor

The high power pulsed radar transistor device part number IB2931MH155 is designed for S-Band radar systems operating over the instantaneous bandwidth of 2.9-3.1 GHz. While operating in class C mode this common base device supplies a minimum of 155 watts of peak pulse power under the conditions of 100µs pulse width and 10% duty cycle over the frequency range of 2.9-3.1 GHz. All devices are 100% screened for large signal RF parameters, including power gain compression. Excellent spectral stability into output mismatch over a broad input power range make it ideal for use in reliable high power solid state transmitters. The test fixture includes a passive amplitude sloping network to insure that the device is not overdriven as the operating frequency decreases.



Silicon Bipolar

- Ultra-high f_T

Class C Operation

- High Efficiency

Common Base Configuration

- Single Power Supply

Gold Metal

- Maximum Reliability

Emitter Ballasting

- Optimum Thermal Distribution

Internal Impedance Matching

- Ease of Use
- Ultra-low Loss Design

Be0 Package

- Unmatched Thermal Reliability
- Solder Seal Hermeticity

RF Test Fixture

- Broadband
- Matched to 50Ω
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning Allowed
- Micro-strip structure on soft pc board with dielectric constant 10.2

Patents Issued

- US 6181200 B1
- US 6331931 B1

TYPICAL DATA TYPICAL DATA TYPICAL DATA TYPICAL DATA

| | Freq (GHz) | P _{IN} (W) | IRL (dB) | P _{OUT} (W) | G _P (dB) | OPC (dB) | OPF (dB) | I _c (A) | n _c (%) | Droop (dB) | Droop (P-F) | VSWR-S 1.5:1 | LMT 2:1 |
|----------------------|---------------|------------------------|-------------|-------------------------|------------------------|-------------|-------------|-----------------------|-----------------------|---------------|----------------|-----------------|------------|
| OPC | 2.900 | 26.9 | -- | 183 | -- | 0.12 | -- | -- | -- | -- | -- | -- | -- |
| Nominal | 2.900 | 24.0 | -14 | 178 | 8.7 | -- | 0.20 | 12.12 | 41 | -0.50 | P | -- | P |
| 1.5:1 Stability / OD | 2.900 | 28.2 | -- | -- | -- | -- | -- | -- | -- | -- | -- | S | -- |
| OPC | 3.000 | 26.9 | -- | 187 | -- | 0.20 | -- | -- | -- | -- | -- | -- | -- |
| Nominal | 3.000 | 24.0 | -14 | 179 | 8.7 | -- | -- | 11.70 | 42 | -0.45 | P | -- | P |
| 1.5:1 Stability / OD | 3.000 | 28.2 | -- | -- | -- | -- | -- | -- | -- | -- | -- | S | -- |
| OPC | 3.100 | 26.9 | -- | 177 | -- | 0.15 | -- | -- | -- | -- | -- | -- | -- |
| Nominal | 3.100 | 24.0 | -16 | 171 | 8.5 | -- | -- | 10.85 | 44 | -0.29 | P | -- | P |
| 1.5:1 Stability / OD | 3.100 | 28.2 | -- | -- | -- | -- | -- | -- | -- | -- | -- | S | -- |

PW=100us, Duty=10%, Vcc=36V

MAXIMUM RATINGS

| Screen | Parameter | Symbol | Min | Max | Units | Test Conditions |
|--------|--|-----------|-----|------|-------|-----------------|
| BD | Collector-Emitter Voltage | V_{CES} | -- | 70 | V | -- |
| BD | Storage Temperature Range | T_{STG} | -55 | +200 | °C | -- |
| BD | Operating Junction Temperature Range | T_J | -55 | +200 | °C | -- |
| Note | Screen 'BD' = parameter qualified By Design. | | | | | |

THERMAL CHARACTERISTICS

| Screen | Parameter | Symbol | Min | Max | Units | Test Conditions |
|--------|--|--------------|-----|------|-------|--|
| BD | Thermal Resistance | $R_{TH(JC)}$ | | 0.25 | °C/W | $V_{CC}=V1$, $PW=PW1$, $DF=DF1$, $T_F=25\pm5^\circ C$, $P_{OUT}=155W$, $N_C=38\%$. |
| Note | Screen 'BD' = parameter qualified By Design. | | | | | |

PROCESSING SPECIFICATIONS

| Screen | Parameter | Symbol | Min | Max | Units | Test Conditions |
|--------|--|--------|-----|-----|-------|---|
| 100% | DC Wafer Probe | -- | -- | -- | -- | Per Integra specification. |
| Q1 | Wafer DC and RF Qualification | -- | -- | -- | -- | Per Integra specification. |
| LM | Wire Bond Strength | -- | -- | -- | -- | Line monitor per Integra specification. |
| 100% | Pre-cap visual inspection | -- | -- | -- | -- | Per Integra specification |
| 100% | Gross leak test | -- | -- | -- | -- | MIL-STD-750D, Method 1071, Test Condition C |
| Note | Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer. | | | | | |
| Note | Screen 'LM' = parameter is qualified by assembly line monitor. | | | | | |

DC ELECTRICAL CHARACTERISTICS

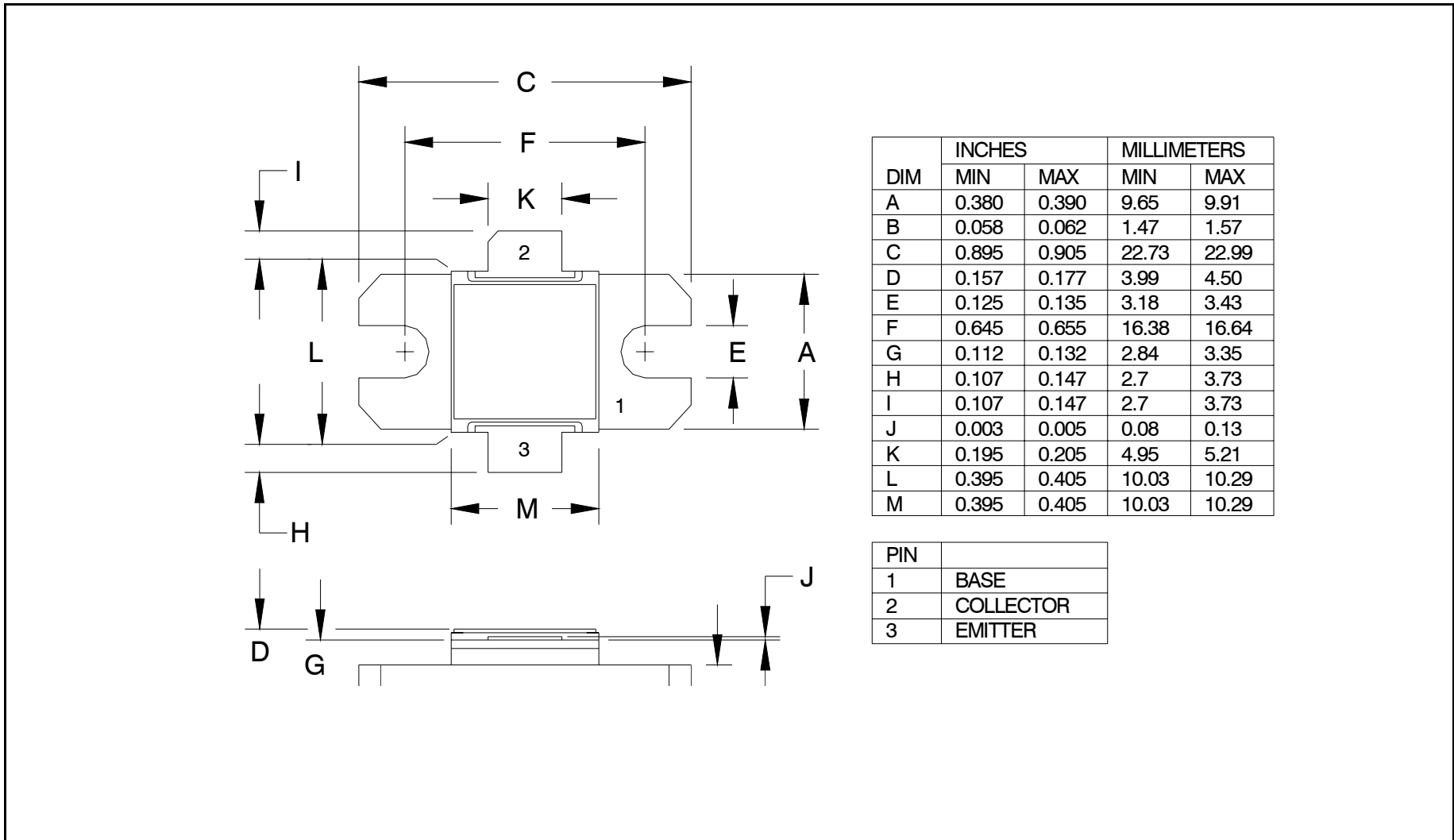
| Screen | Parameter | Symbol | Min | Max | Units | Test Conditions |
|--------|---|------------|-----|-----|-------|---|
| 100% | Collector-Emitter Breakdown Voltage | BV_{CES} | 65 | -- | V | $I_C=30mA$, $V_{BE}=0V$, $T_F=25\pm5^\circ C$. |
| 100% | Zero Base Voltage Collector Leakage Current | I_{CES} | -- | 6.0 | mA | $V_{CE}=30V$, $V_{BE}=0V$, $T_F=25\pm5^\circ C$. |
| 100% | DC Current Gain | H_{FE} | 10 | 120 | -- | $V_{CE}=5V$, $I_C=0.1A$, $T_F=25\pm5^\circ C$. |

RF ELECTRICAL CHARACTERISTICS

| Screen | Parameter | Symbol | Min | Max | Units | Test Conditions |
|--------|--|-----------|-------|-------|-------|---|
| 100% | Input Return Loss | IRL | -- | -7 | dB | $V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, F=F1, F2, F3$ |
| 100% | Output Power | P_{OUT} | 155 | -- | W | $V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, F=F1, F2, F3$ |
| 100% | Collector Efficiency ($P_o/I_c/V_{CC}$) | N_c | 38 | -- | % | $V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, F=F1, F2, F3$ |
| 100% | Pulse Amplitude Droop | D | -- | 0.70 | dB | $V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, F=F1, F2, F3$ |
| 100% | Output Power Compression = $10*\text{LOG}(P_{OC}/P_o)$ | OPC | +0.02 | +0.48 | dB | P_{OC} measured with P_{IN} increased by 0.5dB at $F=F1, F2, F3$ |
| 100% | Output Power Flatness = $10*\text{LOG}(P_{OMAX}/P_{OMIN})$ | OPF | -- | 0.75 | dB | Calculate from P_o at each frequency $F1, F2, F3$. |
| 100% | Delta Insertion Phase Variation | d-IP | -30 | +30 | Deg | $V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN3}, F=F2$, Mark in 5° increments. See note 3. |
| 100% | Stability into 1.5:1 VSWR with +0.7dB overdrive | VSWR-S | -- | -- | -- | $V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, P_{IN2}, P_{IN3}, F=F1, F2, F3$. Repeat P_o with P_{IN} increased by 0.70dB. Rotate 1.5:1 output VSWR through 360° of phase. No oscillatory or pulse break-up characteristics are allowed on the detected output pulse. All non-harmonically related signals must be at least -65 dBc. |
| 100% | 2:1 Load Mismatch Tolerance | LMT | -- | -- | -- | $V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, P_{IN2}, P_{IN3}, F=F1, F2, F3$. Rotate 2:1 output VSWR through 360° of phase. Post test $P_o = \text{Pre test } P_o \pm 5W$. |
| BD | Risetime | RT | -- | 150 | ns | $V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, F=F1, F2, F3$ Measure at 10 & 90% detected power points. |
| Note 1 | $V1 = 36V; PW1 = 100\mu s; DF1 = 10\%; P_{IN1} = P_{IN2} = P_{IN3} = 24.0W; F1 = 2.90 \text{ GHz}, F2 = 3.00 \text{ GHz}, F3 = 3.10 \text{ GHz}$. | | | | | |
| Note 2 | $T_F = \text{Device flange temperature}$. Screen 'BD' = parameter qualified By Design. | | | | | |
| Note 3 | Parts are binned and marked in 5 degree increments for Insertion Phase IP: ITI-1, -2, -3, -4, -5, -6, -7, -8, -9, -10, -11, -12. | | | | | |

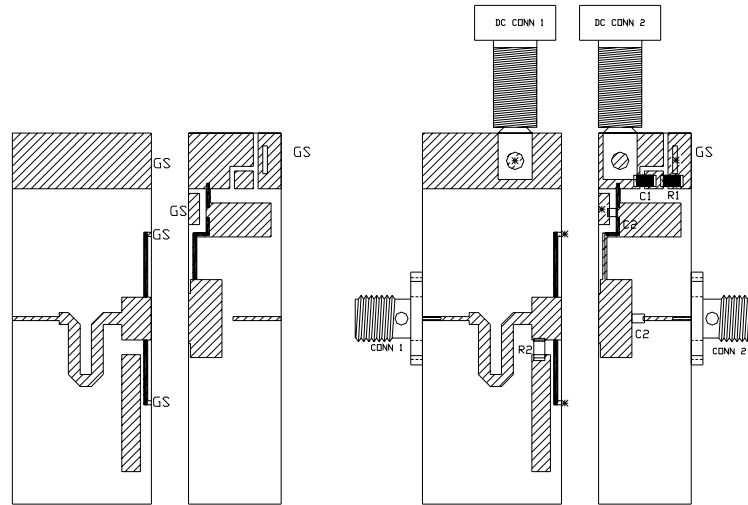
RF TEST FIXTURE IMPEDANCE CHARACTERISTICS

| Frequency (MHz) | $Z_{IF} (\Omega)$ | $Z_{OF} (\Omega)$ |
|----------------------|-------------------|-------------------|
| 2.90 | 4.73 -j6.87 | 2 -j5.5 |
| 3.00 | 4.29 -j5.79 | 2 -j5.2 |
| 3.10 | 4.14 -j4.77 | 1.95 -j4.96 |
| Impedance Definition | | |



PACKAGE DIMENSIONAL OUTLINE DRAWING

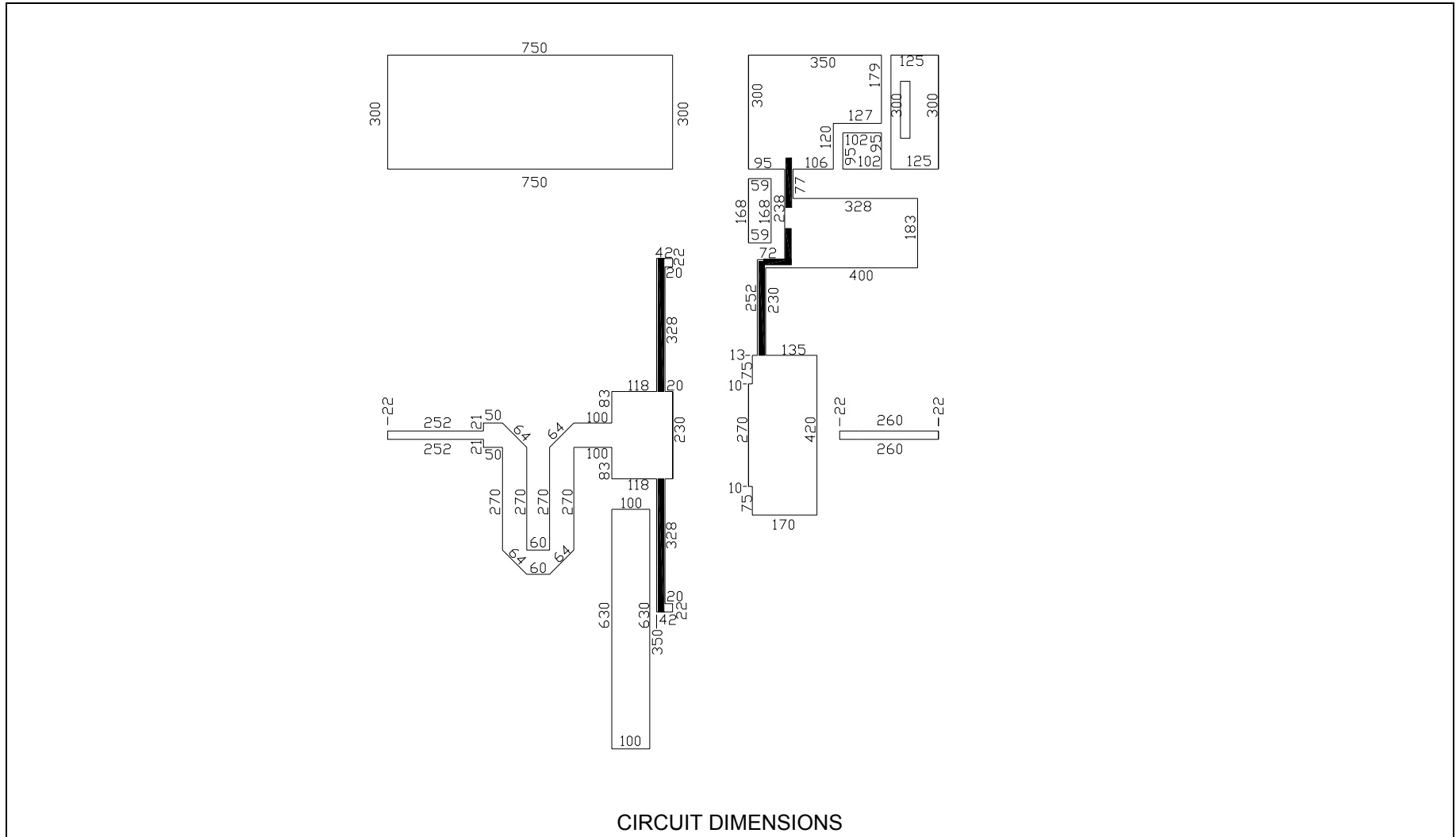
RF TEST FIXTURE



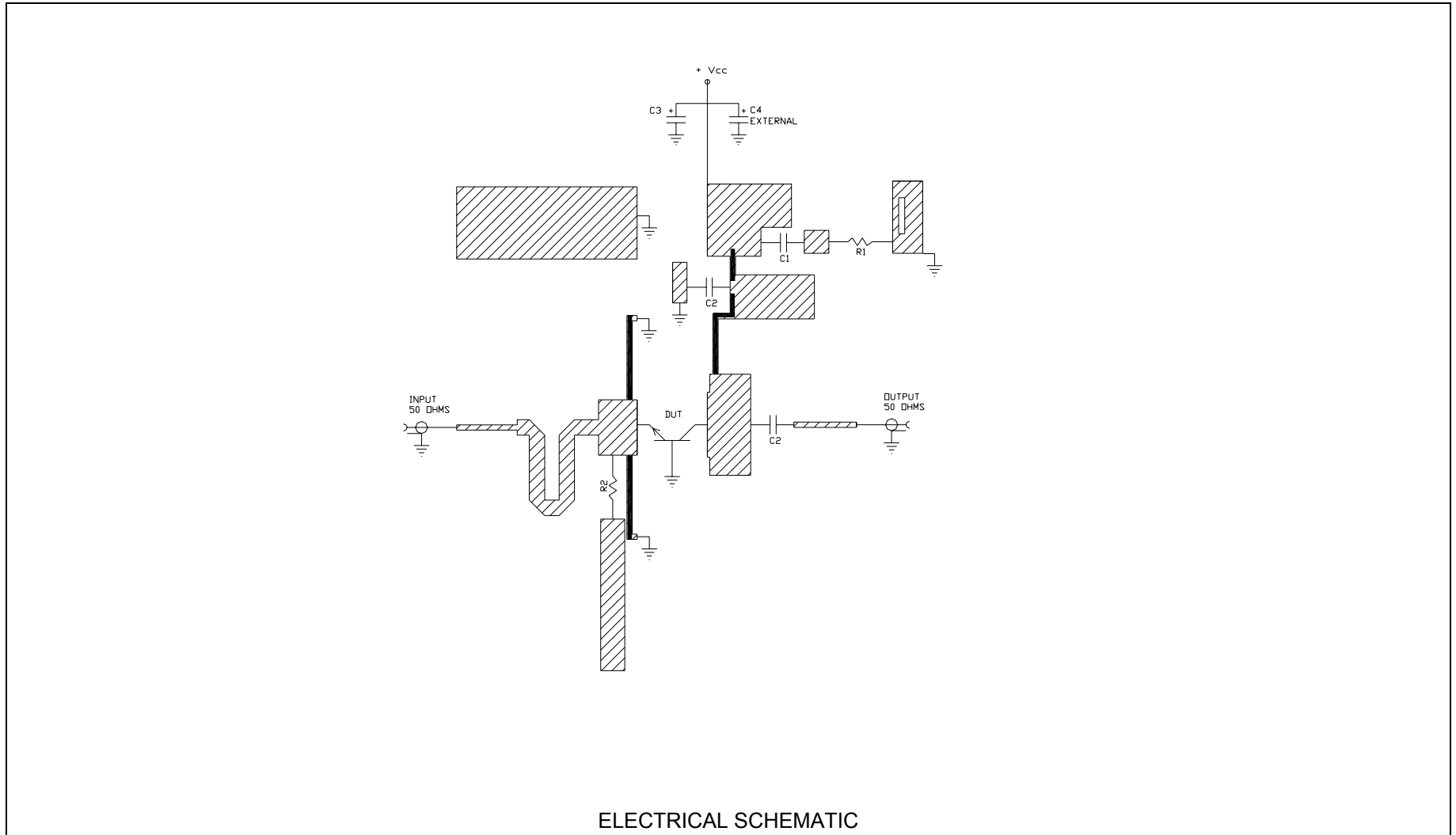
| COMPONENT | DESCRIPTION |
|-------------------------|---|
| DUT | TRANSISTOR #IB2931MH155 MOUNT HARD TO THE RIGHT |
| PC BOARD | ROGERS #R0 6010.2LM 2E/2E .025" |
| C1 | SNUB CAPACITOR 0.1uF |
| C2 | CHIP CAPACITOR ATC100A 39pF |
| C3 | ELECTROLYTIC CAPACITOR 98uF/6.3V |
| C4 (NOT SHOWN) | ELECTROLYTIC CAPACITOR 4700uF / 50V |
| R1 | SNUB RESISTOR 6.81 Ohms |
| R2 | CHIP RESISTOR 51 Ohms |
| BIAS (3 PLACES) | BIAS LINE WIRE |
| GS (5 PLACES) | GROUND SHIM, COPPER, TH=0.001" |
| CONN 1, CONN 2 | SMA CONNECTOR, QS #2052-5636-02 |
| INPUT PC BOARD CARRIER | 2 INCH BRASS-02 (0.75") |
| OUTPUT PC BOARD CARRIER | 2 INCH BRASS-01 (0.5") |
| TRANSISTOR CARRIER | 2 INCH COPPER-02 (P44) |
| TRANSISTOR CLAMP | NDRYL CLAMP-02 (P44) |
| ALUMINUM HEAT SINK | 2 INCH HEATSINK-09 |
| DC CONN 1 | BANANA JACK, BLACK |
| DC CONN 2 | BANANA JACK, RED |
| NOTE | FIXTURE HARDWARE DRAWINGS AVAILABLE ON REQUEST |

ASSEMBLY AND PARTS LIST

RF TEST FIXTURE



RF TEST FIXTURE



ELECTRICAL SCHEMATIC

DEFINITIONS

| Data Sheet Status | |
|---|---|
| Proposed Specification | This data sheet contains proposed specifications. |
| Preliminary Specification | This data sheet contains specifications based on preliminary measurements and data. |
| Product Specification | This data sheet contains final product specifications. |
| Maximum Ratings | |
| Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only. Operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability. | |

WARNING

| Product and environmental safety - toxic materials |
|--|
| This product contains beryllium oxide. The product is entirely safe provided that the BeO base is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with general or domestic waste. |

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