

S-Band Radar Transistor

Part number ILD2731M30 is designed for S-Band radar applications operating over the 2.7-3.1 GHz instantaneous frequency band. Under 300us/10% pulsing conditions it easily supplies a minimum of 30 watts of peak output power with well over 10dB gain. Since it operates under Class B or AB bias it exhibits a fairly linear Pin versus Pout transfer characteristic, which allows operation at reduced output power levels. With appropriate rating, it is operable under nearly any pulse width and duty factor condition. It operates with spectral purity into output VSWR with simultaneous input power overdrive. All devices are 100% screened for large signal RF parameters in a fixed tuned broadband matching circuit / test fixture. The use of external tuners is not allowed during screening.



Silicon LDMOS FET

- High Power Gain
- Excellent thermal stability
- Gold Metal

Gold Metal System

- Complete Gold System
- LDMOS with Gold Metal
- Gold Bond Wires
- Gold Package Metal
- Maximum Reliability

Class B, AB or A Operation

- Minimal Quiescent Current in Class B mode
- Linearized Transfer Characteristic

Internal Impedance Matching

- Ease of Use
- Ultra Low Loss Design

BeO Free Package

- Metal Based
- Epoxy Seal

High Power RF Test / Fixture

- Broadband
- Matched to 50 Ω (ohms)
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning required

TYPICAL DATA TYPICAL DATA TYPICAL DATA TYPICAL DATA

FREQ (GHz)	PIN (W)	IRL (dB)	P _{OUT} (W)	G _P (dB)	I _D (A)	OPF (dB)	Droop (dB)	VSWR-S 3:1	VSWR-S 3:1
2.70	2.0	-14.58	40.66	13.08	3.02	0.18	-0.25	S	P
2.90	2.0	-11.25	40.56	13.07	2.82		-0.15	S	P
3.10	2.0	-11.85	42.27	13.25	2.94		-0.18	S	P

MAXIMUM RATINGS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Drain-Source Voltage	V_{DS}	--	65	V	--
BD	Gate-Source Voltage	V_{GS}	-0.5	12	V	--
BD	Storage Temperature Range	T_{STG}	-55	+150	°C	--
BD	Operating Junction Temperature Range	T_J	-55	+200	°C	--
Note	Screen 'BD' = parameter qualified By Design.					

THERMAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	1.2	°C/W	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{OUT}=30W, F=F3$
Note	Screen 'BD' = parameter qualified By Design.					

PROCESSING SPECIFICATIONS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071.6, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

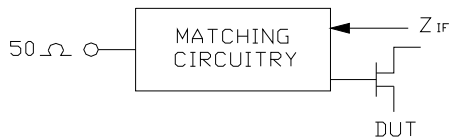
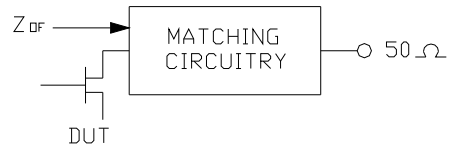
DC ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Drain-Source Breakdown Voltage	BV_{DSS}	65	--	V	$I_{DS}=10mA, V_{GS}=0V, T_F=25\pm5^\circ C$
100%	Drain Leakage Current	I_{DSS}	--	1.0	uA	$V_{DS}=32V, V_{GS}=0V, T_F=25\pm5^\circ C$
100%	Operating Gate Voltage	V_{GS}	2.5	4.0	V	$V_{DS}=5V, I_D=0.1A, T_F=25\pm5^\circ C$
100%	Gate Leakage Current	I_{GSS}	--	1.0	uA	$V_{GS}=10V, V_{DS}=0V, T_F=25\pm5^\circ C$

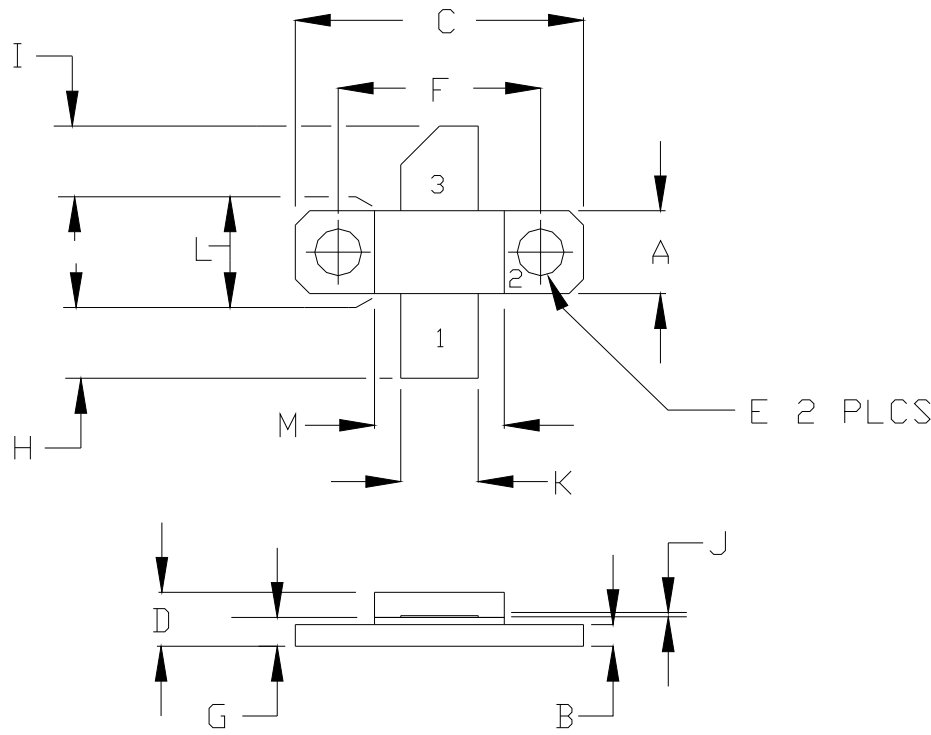
RF ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	IRL	-18	-7	dB	$V_{DD}=V1, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, P_{IN2}, P_{IN3}, F=F1, F2, F3.$
100%	Output Power	P_O	30	55	W	$V_{DD}=V1, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Drain Current Peak	I_D	2.0	4.0	A	$V_{DD}=V1, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, P_{IN2}, P_{IN3}, F=F1, F2, F3.$
100%	Pulse Amplitude Droop	D	-0.50	+0.3	dB	$V_{DD}=V1, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, P_{IN2}, P_{IN3}, F=F1, F2, F3.$
100%	3:1 Load Mismatch Stability & Tolerance with Simultaneous Input Power Overdrive	VSWR-ST	--	--	--	$V_{DD}=V1, PW=PW1, DF=DF1, T_F=T_{F1}, F=F1, F2, F3.$ $P_{IN}=P_{IN1}+0.75dB, P_{IN}=P_{IN2}+0.75dB, P_{IN}=P_{IN3}+0.75dB,$ Rotate 3:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse. All non-harmonically related signals must be at least -65 dBc.
100%	Output Power Flatness (10 Log (Pout Max/Pin Max))	OPF	0	1	dB	$V_{DD}=V1, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, P_{IN2}, P_{IN3}, F=F1, F2, F3.$
100%	Gain	G_p	11.76	14.39	dB	$V_{DD}=V1, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, P_{IN2}, P_{IN3}, F=F1, F2, F3.$
Note 1	$V1 = 32V; I_{DQ1} = 10mA; PW1 = 300us; DF1 = 10\%,$					
Note 2	Input Power Test Levels: $P_{IN1}, P_{IN2}, P_{IN3} = 2.0W$					
Note 3	Test Frequencies: $F1 = 2.70 GHz, F2 = 2.90 GHz, F3 = 3.10 GHz.$					
Note 4	$T_{F1} = 25\pm5^\circ C =$ Device flange temperature.					
Note 5	Screen 'BD' = parameter qualified By Design.					

RF TEST FIXTURE IMPEDANCE CHARACTERISTICS

Frequency (GHz)	$Z_{IF} (\Omega)$	$Z_{OF} (\Omega)$
2.70	2.0 – j5.18	6.7 – j9.1
2.90	1.91 – j4.54	6.3 – j8.2
3.10	2.1 – j4.14	6.2 – j7.67
Impedance Definition		

PACKAGE DIMENSIONAL OUTLINE DRAWING

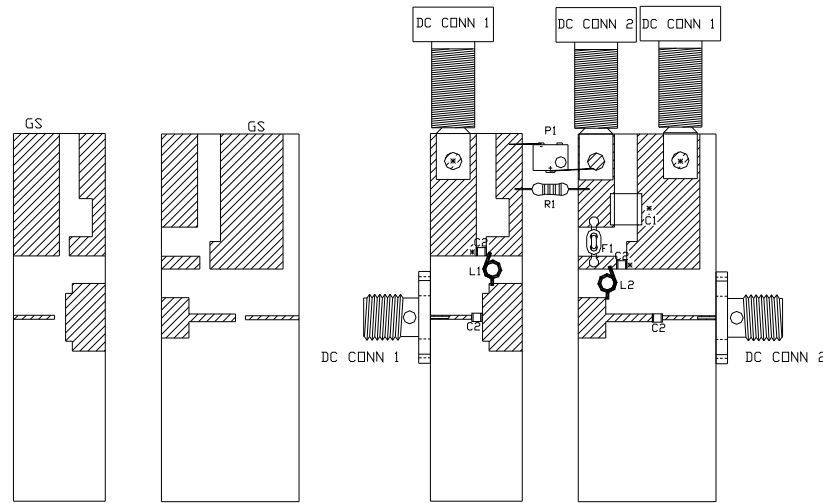


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.225	0.235	5.71	5.96
B	0.055	0.065	1.40	1.65
C	0.795	0.805	20.19	20.44
D	0.140	0.160	3.55	4.06
E	0.125	0.135	3.18	3.43
F	0.557	0.567	14.14	14.40
G	0.077	0.087	1.95	2.20
H	0.215	0.245	5.46	6.22
I	0.215	0.245	5.46	6.22
J	0.004	0.006	0.10	0.15
K	0.210	0.220	5.33	5.58
L	0.225	0.235	5.71	5.96
M	0.355	0.365	9.01	9.27

PIN SCHEDULE	
1	GATE
2	SOURCE
3	DRAIN

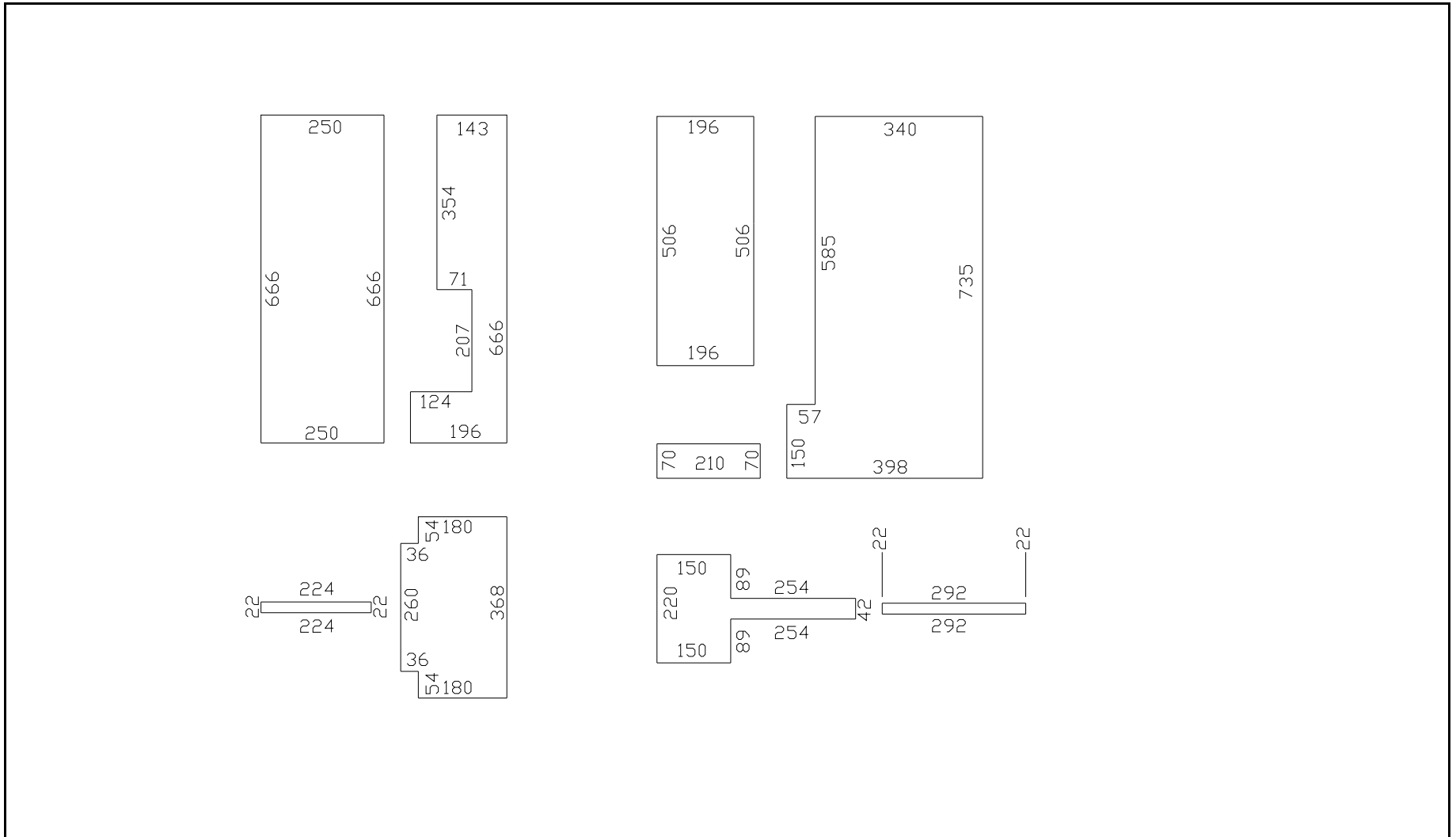
NOTES:
LID: LID-PL32-1

RF TEST FIXTURE – ASSEMBLY AND PARTS LIST

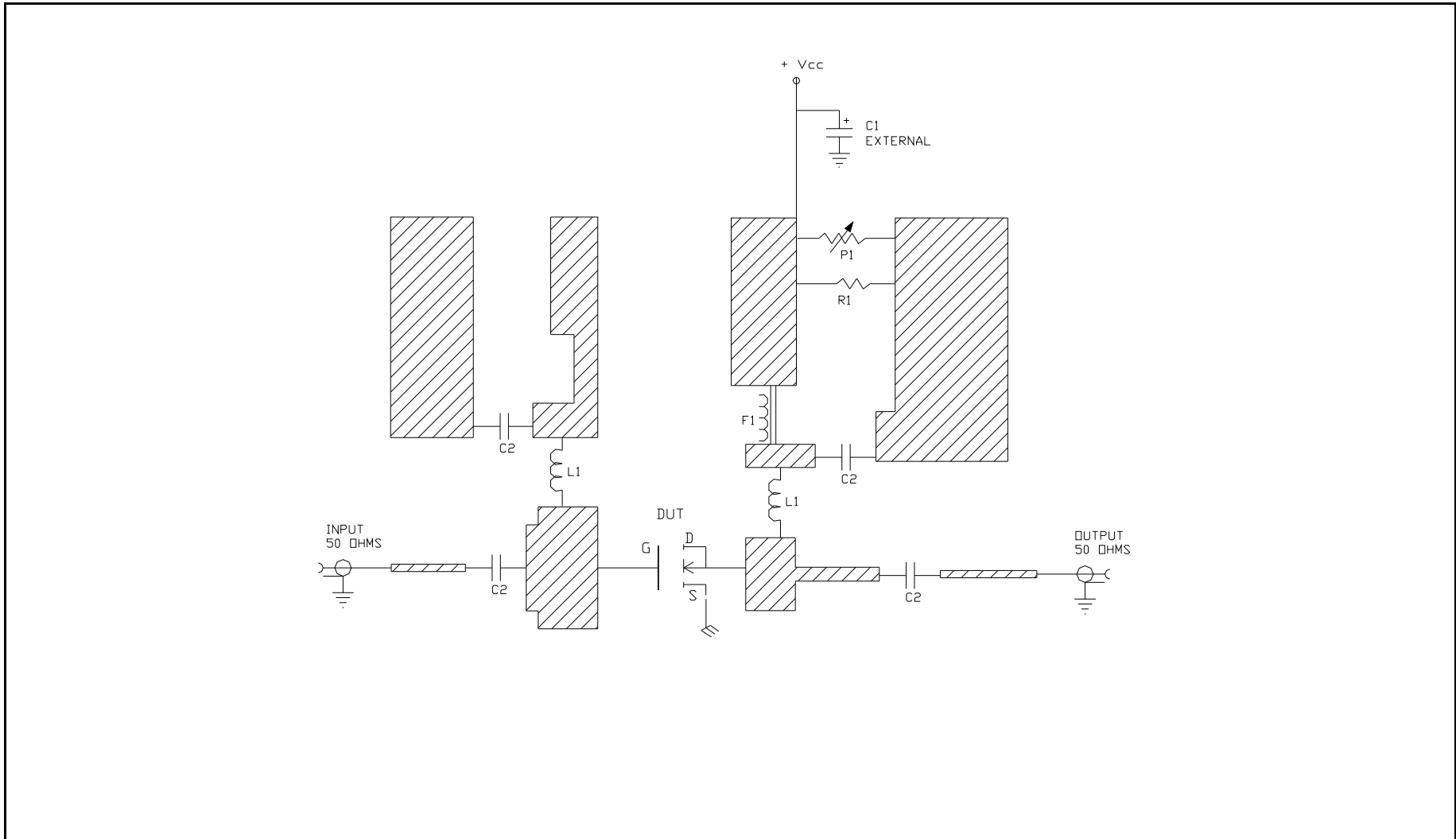


COMPONENT	DESCRIPTION
DUT	TRANSISTOR ILD2731M30 MOUNT HARD TO THE RIGHT
PC BOARD	ROGERS #RD 6010.2 1oz. Cu. 25 MILS THICK
C1(NOT SHOWN EXTERNAL)	ELECTROLYTIC CAPACITOR 4.7uF / 50V
C2	CAPACITOR CHIP ATC100A, 39pF (4 PLACES)
L1	COIL: 2 TURN AWG#22 INSULATED, .076" DIA, PULL TIGHT AND FULLY CLOSED, LEFT HAND.
L2	COIL: 2 TURN AWG#22 INSULATED, 0.76" DIA, PULL TIGHT AND FULLY CLOSED, RIGHT HAND.
F1	FERRITE TWIN HOLE CORE, FERRONICS PN#12-315-J
R1	1 TURN AWG# 22 INSULATED.
P1	POTENTIOMETER
BIAS LINE WIRE	BIAS LINE WIRE (1 PLACE)
GS (4 PLACES)	GROUND SHIM, COPPER, TH=0.001"
CONN 1, CONN 2	SMA CONNECTOR, DS #2052-5636-02
INPUT PC BOARD CARRIER	2 INCH BRASS-01 (0.50")
OUTPUT PC BOARD CARRIER	2 INCH BRASS-01 (0.50")
TRANSISTOR CARRIER	2 INCH COPPER-01 (P32)
TRANSISTOR CLAMP	NDRYL CLAMP-01 (P32)
ALUMINUM HEAT SINK	2 INCH HEATSINK-09
DC CONN 1	BANANA JACK, BLACK
DC CONN 2	BANANA JACK, RED
NOTE	FIXTURE HARDWARE DRAWINGS AVAILABLE ON REQUEST

RF TEST FIXTURE – CIRCUIT DIMENSIONS



RF TEST FIXTURE – ELECTRICAL SCHEMATIC



DEFINITIONS

Data Sheet Status	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
Maximum Ratings	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

WARNING

Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO base is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with general or domestic waste.

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