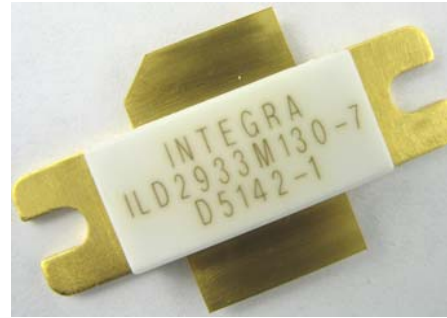


S-Band Radar Transistor

Part number ILD2933M130 is designed for S-Band radar applications operating over the 2.9 – 3.3 GHz instantaneous frequency band. Under 300us / 10% pulsing conditions it supplies a minimum of 130 watts of peak output power with 11dB gain typically. Specified operation is with Class AB bias. The broadband test fixture includes a temperature compensated bias network. All devices are 100% screened for large signal RF parameters in a fixed tuned broadband matching circuit / test fixture. The use of external tuners is not allowed during screening.



Silicon LDMOS FET

- High Power Gain
- Excellent thermal stability
- Gold Metal

Gold Metal System

- Complete Gold System
- LDMOS with Gold Metal
- Gold Bond Wires
- Gold Package Metal
- Maximum Reliability

Class AB Operation

- Specified with AB bias

Internal Impedance Matching

- Ease of Use
- Ultra Low Loss Design

BeO Free Package

- Metal Based
- Epoxy Seal

High Power RF Test / Fixture

- Broadband
- Matched to 50 Ω (ohms)
- Temperature Compensated Bias
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning required

TYPICAL DATA TYPICAL DATA TYPICAL DATA TYPICAL DATA

FREQ (GHz)	PW (us)	Duty (%)	V _{DD} (V)	I _{DQ} (mA)	P _{IN} (W)	IRL (dB)	P _{OUT} (W)	G _P (dB)	I _D (A)	N _D (%)	Droop (dB)	VSWR-S 3:1
2.9	300	10	32	50	12	-16	175	11.6	12.18	45	-0.26	Pass
3.1	300	10	32	50	12	-8	174	11.6	12.62	43	-0.31	Pass
3.3	300	10	32	50	12	-12	158	11.2	11.23	44	-0.19	Pass

MAXIMUM RATINGS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Drain-Source Voltage	V_{DS}	--	65	V	--
BD	Gate-Source Voltage	V_{GS}	-0.5	12	V	--
BD	Storage Temperature Range	T_{STG}	-55	+150	°C	--
BD	Operating Junction Temperature Range	T_J	-55	+200	°C	--
Note	Screen 'BD' = parameter qualified By Design.					

THERMAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	0.17	°C/W	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{OUT}=120W, N_D=40\%$
Note	Screen 'BD' = parameter qualified By Design.					

PROCESSING SPECIFICATIONS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071.6, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					



DC ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Drain-Source Breakdown Voltage	BV_{DSS}	65	--	V	$I_{DS}=10mA, V_{GS}=0V, T_F=25\pm5^\circ C$
BD	Drain Leakage Current	I_{DSS}	--	1.0	uA	$V_{DS}=32V, V_{GS}=0V, T_F=25\pm5^\circ C$
100%	Operating Gate Voltage	V_{GS}	2.5	4.0	V	$V_{DS}=5V, I_D=0.1A, T_F=25\pm5^\circ C$
BD	Gate Leakage Current	I_{GSS}	--	1.0	uA	$V_{GS}=10V, V_{DS}=0V, T_F=25\pm5^\circ C$

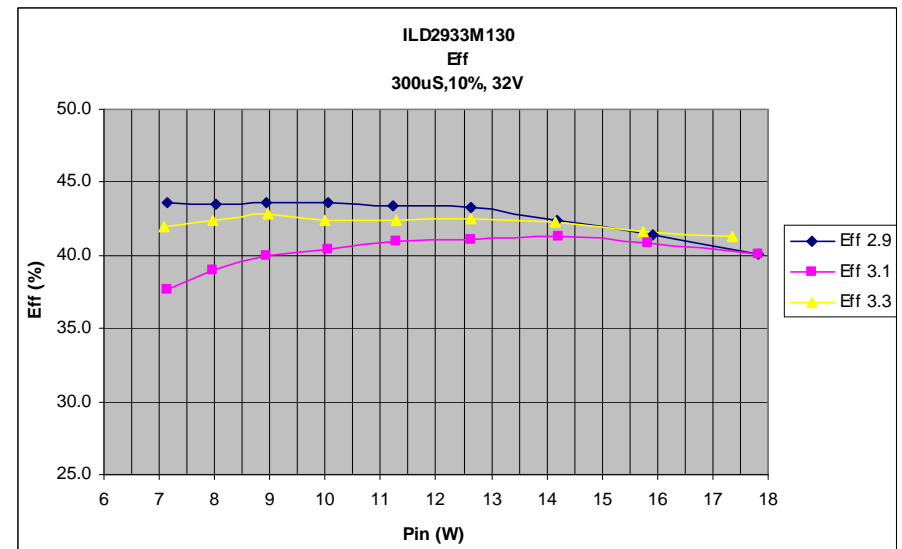
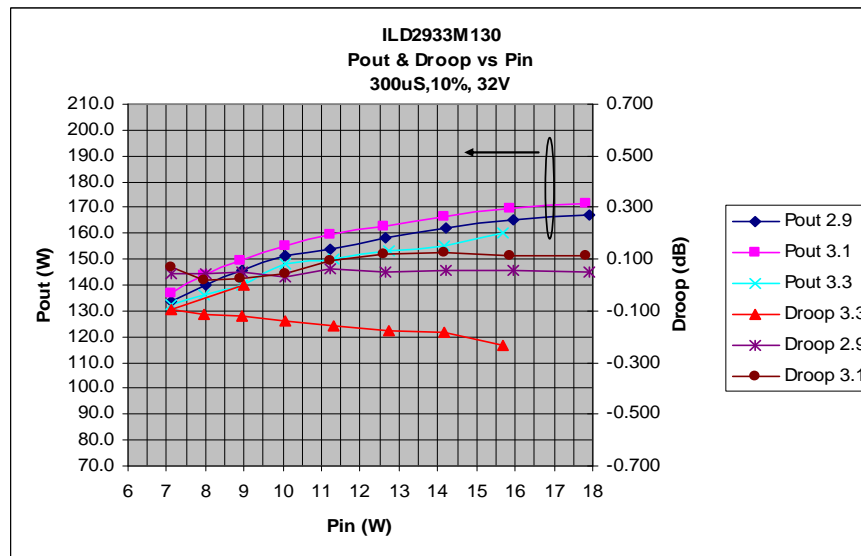
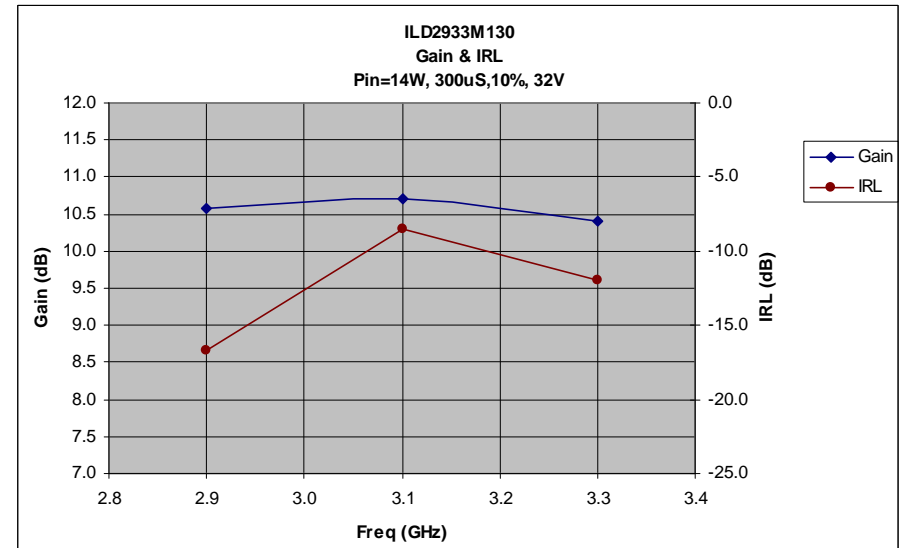
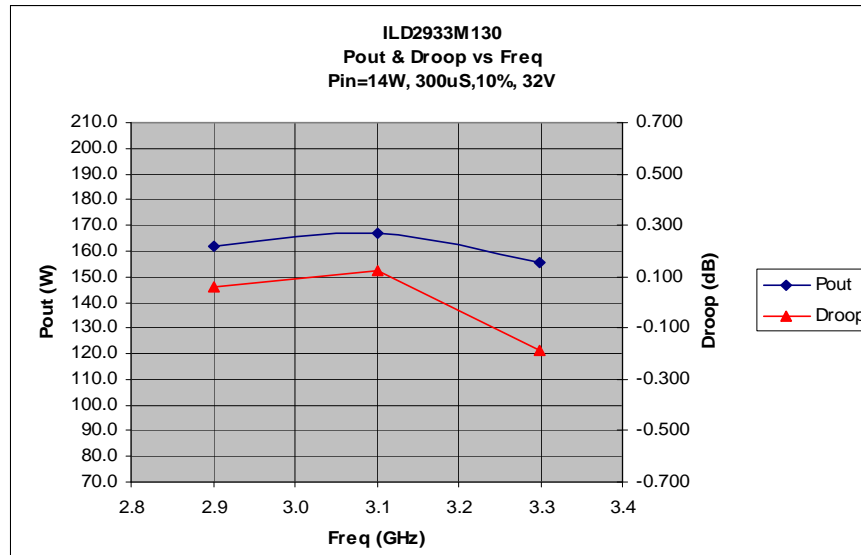
RF ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	IRL	-18	-7	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Output Power	P_O	130	200	W	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Drain Efficiency	N_D	40	50	%	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	Pulse Amplitude Droop	D	-0.50	+0.50	dB	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$
100%	3:1 Load Mismatch Stability	VSWR-S	--	--	--	$V_{DD}=V1, I_{DQ}=I_{DQ1}, PW=PW1, DF=DF1, T_F=T_{F1}, P_{IN}=P_{IN1}, F=F1, F2, F3.$ Rotate 3:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse. All non-harmonically related signals must be at least -65 dBc.
Note 1	$V1 = 32V; I_{DQ1} = 50mA; PW1 = 300\mu s; DF1 = 10\%, P_{IN1} = 12W.$					
Note 2	Test Frequencies: $F1 = 2.9\text{ GHz}, F2 = 3.1\text{ GHz}, F3 = 3.3\text{ GHz}.$					
Note 3	$T_{F1} = 25\pm 5^\circ\text{C} = \text{Device flange temperature}.$					
Note 4	Screen 'BD' = parameter qualified By Design.					

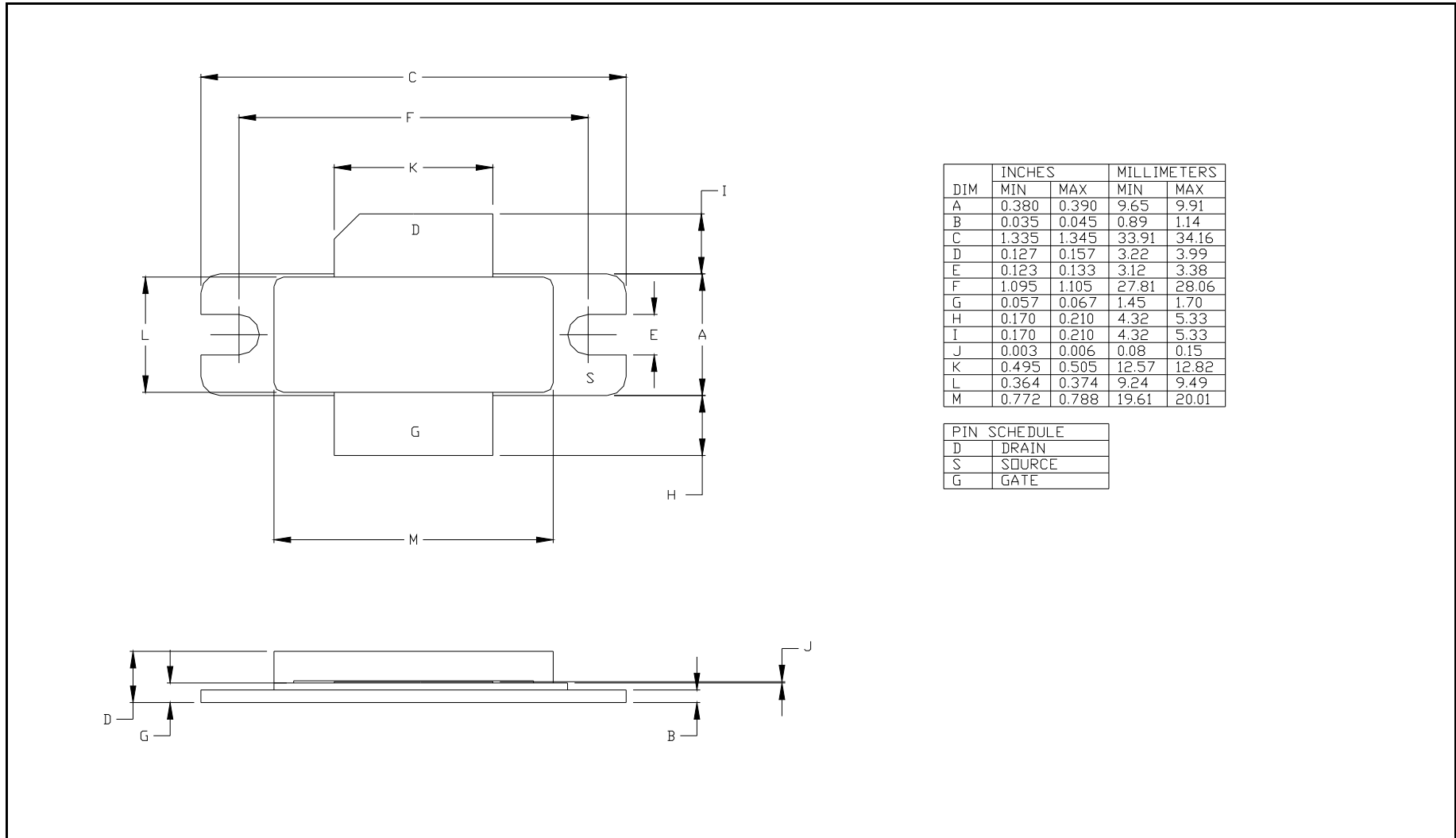
RF TEST FIXTURE IMPEDANCE CHARACTERISTICS

Frequency (GHz)	$Z_{IF} (\Omega)$	$Z_{OF} (\Omega)$
2.90	3.3 - j 5.6	2.6 - j 4.0
3.10	3.4 - j 4.8	2.5 - j 3.0
3.30	3.3 - j 3.9	2.5 - j 1.6
Impedance Definition		

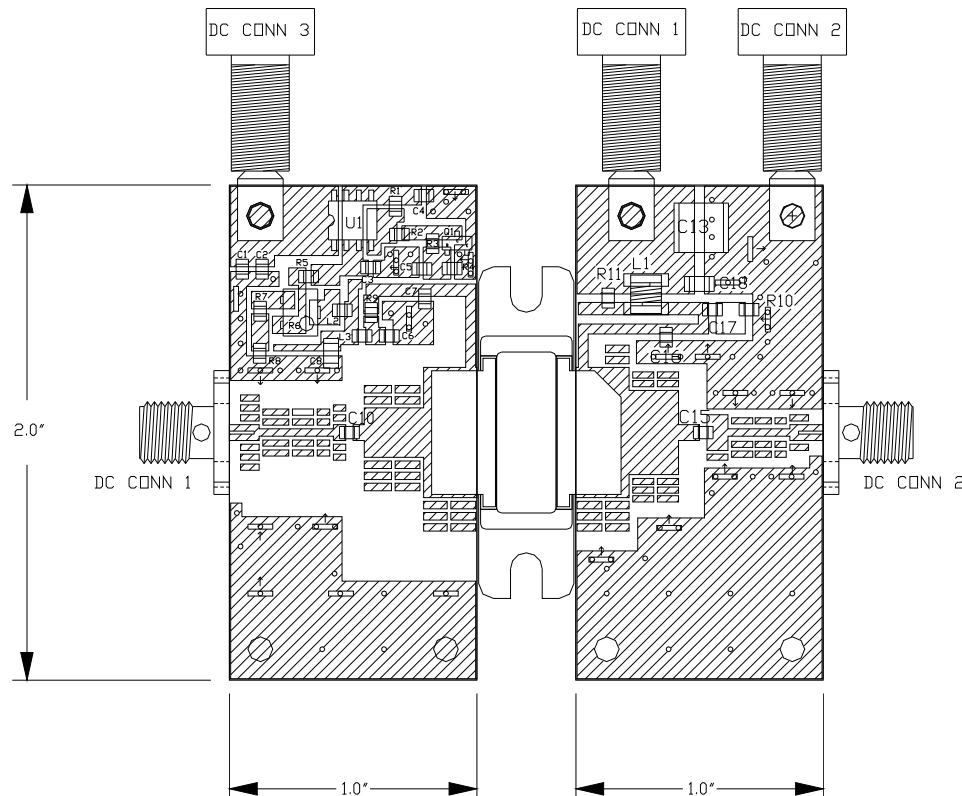
PERFORMANCE GRAPHS



PACKAGE DIMENSIONAL OUTLINE DRAWING



RF TEST FIXTURE – ASSEMBLY AND PARTS LIST

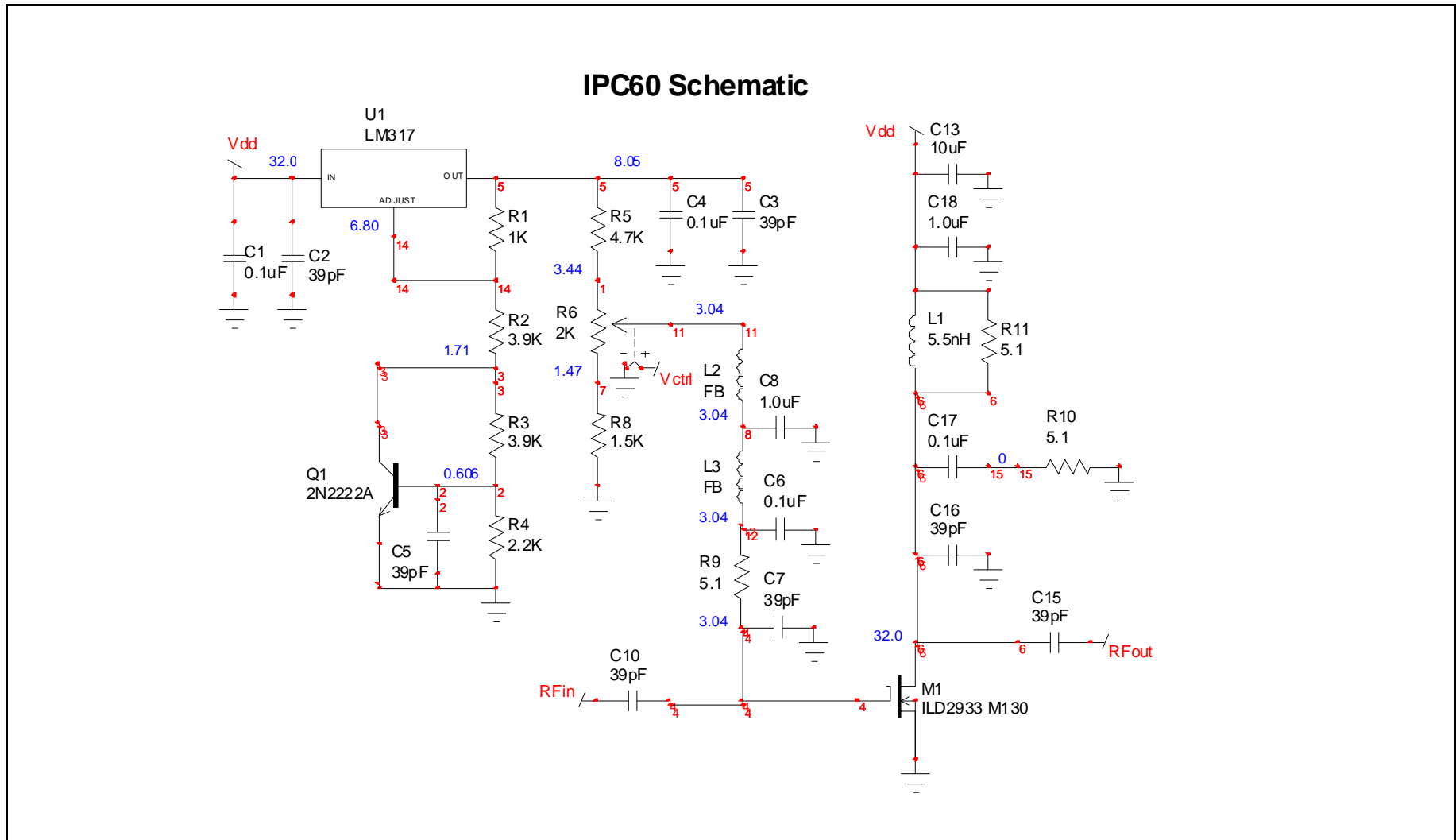


COMPONENT	DESCRIPTION
DUT	TRANSISTOR #ILD2933M130 MOUNT HARD TO THE RIGHT
PC BOARD	ROGER #RD4350B-03011, 30mil 1/1oz Copper
C1, C4, C6, C17	CAPACITOR 0.1uF , 0805 , 50V
C2, C3, C5, C9	CAPCITDR 39pF , ATC600F390C
C7, C10, C15, C16	CAPCITDR 39pF , ATC600F390C EDGE MNT
C8, C18	CAPACITOR 1uF , 1206 , 100V
C13	CAPACITOR 10uF , 2220, 50V , X7R
C14	ALUMINUM ELECTROLYTIC 4700uF , 50V
L1	IND , 5V5.1508
L2, L3	IND , FB , 120 DHM, 0805, 5A
U1	IC , VREG-ADJ.SD1C-8JLM317LM-ND
Q1	PMBT2222
R1	RESISTDR , 1K, 0805
R2, R3	RESISTDR , 3.9K 0805
R4	RESISTDR , 2.2K, 0805
R5	RESISTDR , 4.7K, 0805
R8	RESISTDR , 1.5K, 0805
R7, R9, R10, R11	RESISTDR , 5R1, 0805
R6	RESISTDR , VAR, 2K, 4MM, 3224V, BURNS
GS-GS23	GROUND STRAP, FOLD AS SHOWN GS CAN BE USED INSTEAD OF PLATED VIAS
GS (PLATED THRU VIAS)	GROUND SHIM, COPPER TH=0.001
CONN 1, CONN 2	SMA CONNECTDR, DS #2052-5636-02
INPUT PCB CARRIER	2 INCH BRASS -3 (1')
OUTPUT PCB CARRIER	2 INCH COPPER -22
TRANSISTDR CLAMP	NDRYL CLAMP -08
ALUMINUM HEAT SINK	2 INCH HEAT SINK -11
DC DNN 1	BANANA JACK, RED
DC CONN 2	BANANA JACK, BLACK
DC CONN 3	BANANA JACK, BLUE
DUT	FIXTURE HARDWARE DRAWINGS AVAILABLE ON REQUEST

CONTACT FACTORY FOR RF TEST FIXTURE CAD DRAWING WITH CIRCUIT DIMENSIONS

<L:\Public\Controlled Documents\Controlled Drawings\RF Test Fixture Drawings\ILD2933M130 RF TEST FIXTURE REV PR1.dwg>

RF TEST FIXTURE – ELECTRICAL SCHEMATIC



DEFINITIONS

Data Sheet Status	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
Maximum Ratings	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

WARNING

Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO base is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with general or domestic waste.

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